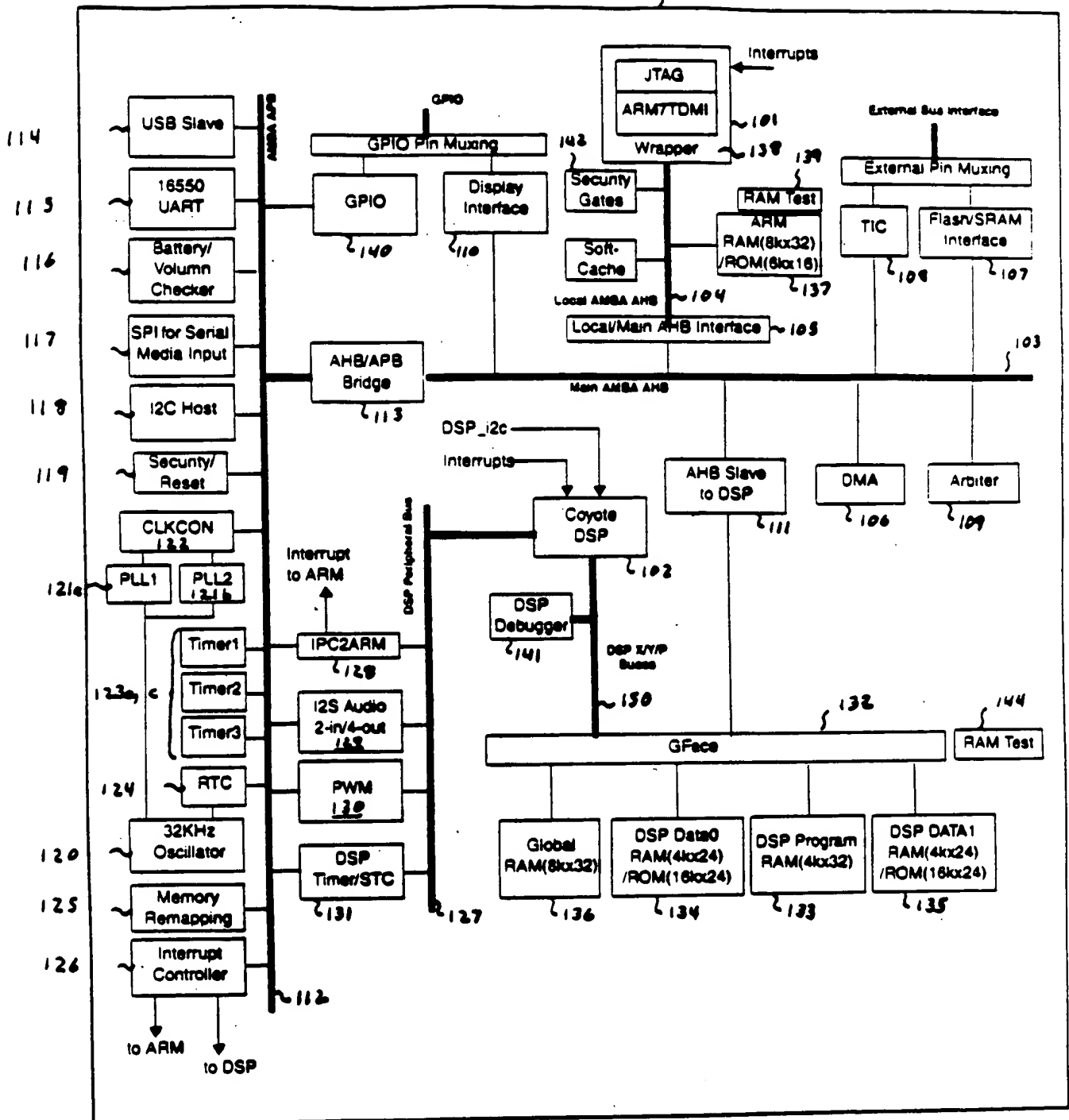
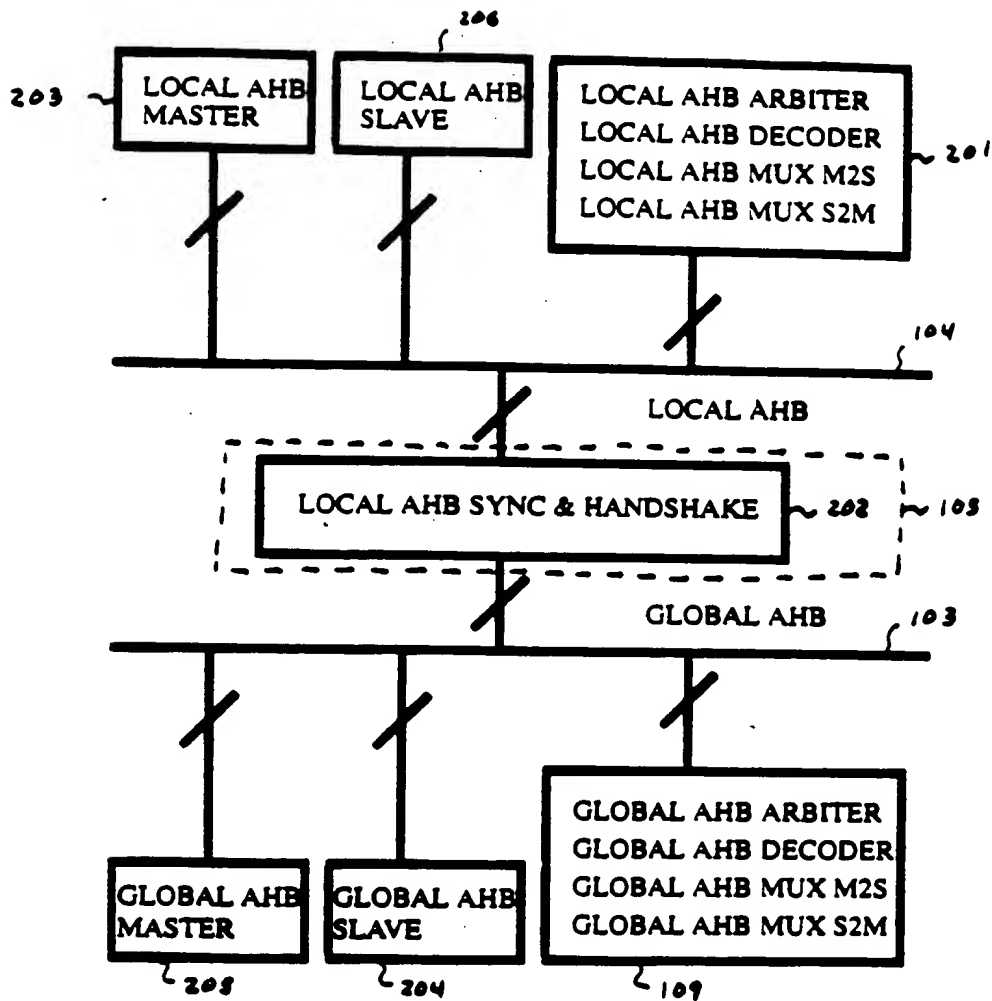


FIG. 1



2836-P139US

FIG. 2A



The diagram shows the timing of various signals relative to the GHCLK domain. The signals are:

- GHCLK**: Global clock signal.
- LHCLK**: Local clock signal.
- LHADDR**: Local address bus, showing addresses A0, A1, A2, and A3.
- LHTRANS**: Local address bus transfer signal.
- LHREADY**: Local address bus ready signal.
- LRDATA**: Local read data bus, showing data D0, D1, D2, and D3.
- LWDATA**: Local write data bus, showing data D0, D1, D2, and D3.
- GHADDR**: Global address bus, showing addresses A0, A1, A2, and A3.
- GHREADY**: Global address bus ready signal.
- GRDATA**: Global read data bus, showing data D0, D1, D2, and D3.
- GWDATA**: Global write data bus, showing data D0, D1, D2, and D3.
- GHSELabbif**: Global select address bus, showing address A0.
- GHSELabbif_reg**: Global select address bus register.
- LHBUSREQabbif**: Local bus request address bus, showing address A0.
- LHGRANT**: Local grant address bus, showing address A0.

The diagram illustrates the relationship between address pushes and data receptions across these signals. The address bus (LHADDR) is pushed into the GHCLK domain, and the data bus (LRDATA, LWDATA) is received in the GHCLK domain. The global address bus (GHADDR) is also pushed into the GHCLK domain, and the global data bus (GRDATA, GWDATA) is received in the GHCLK domain. The global select address bus (GHSELabbif) is pushed into the GHCLK domain, and the global select address bus register (GHSELabbif_reg) is received in the GHCLK domain. The local bus request address bus (LHBUSREQabbif) is pushed into the GHCLK domain, and the local grant address bus (LHGRANT) is received in the GHCLK domain.

FIG. 2B

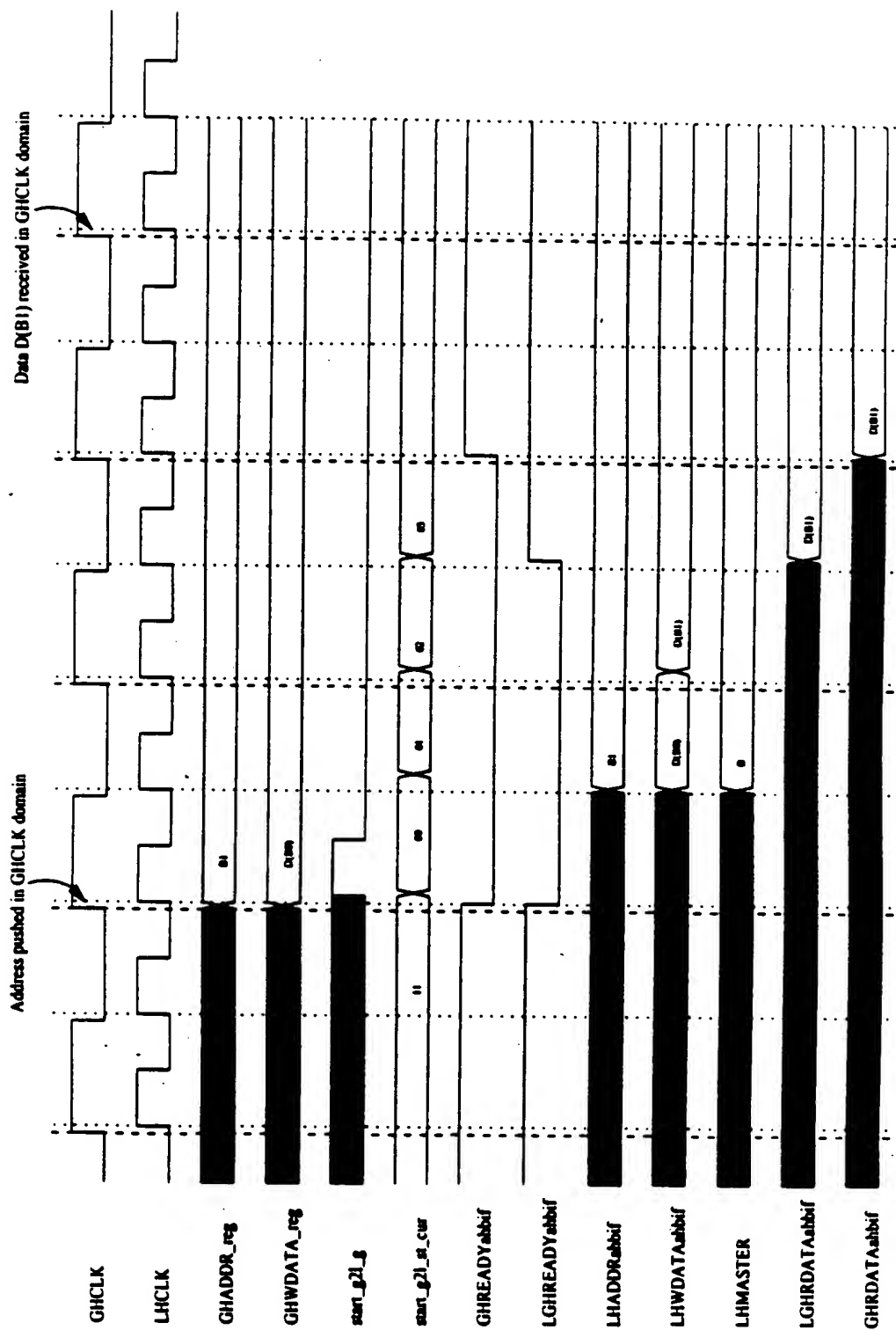


FIG. 2C

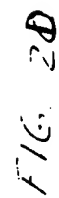


FIG. 2D

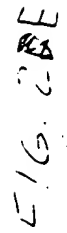
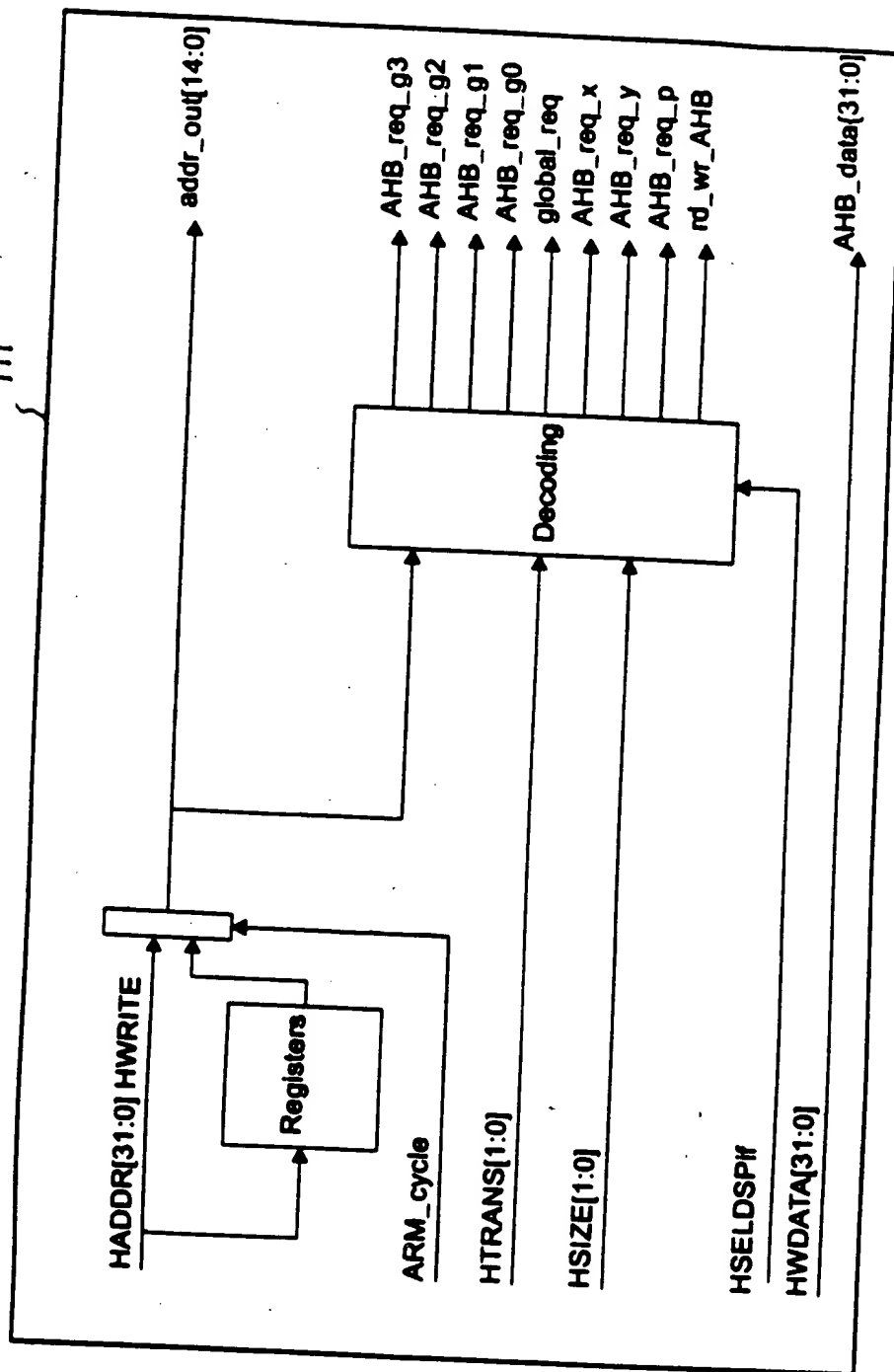


FIG. 3



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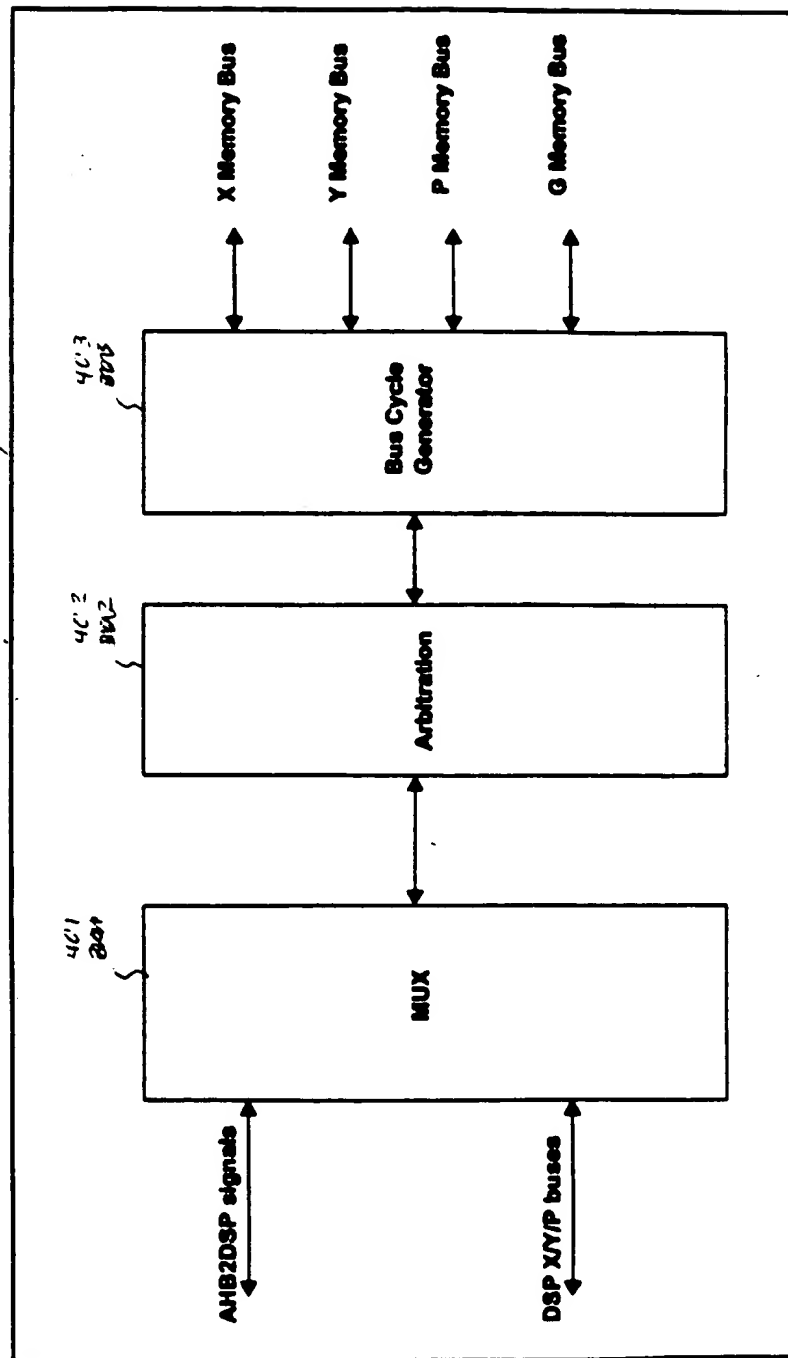
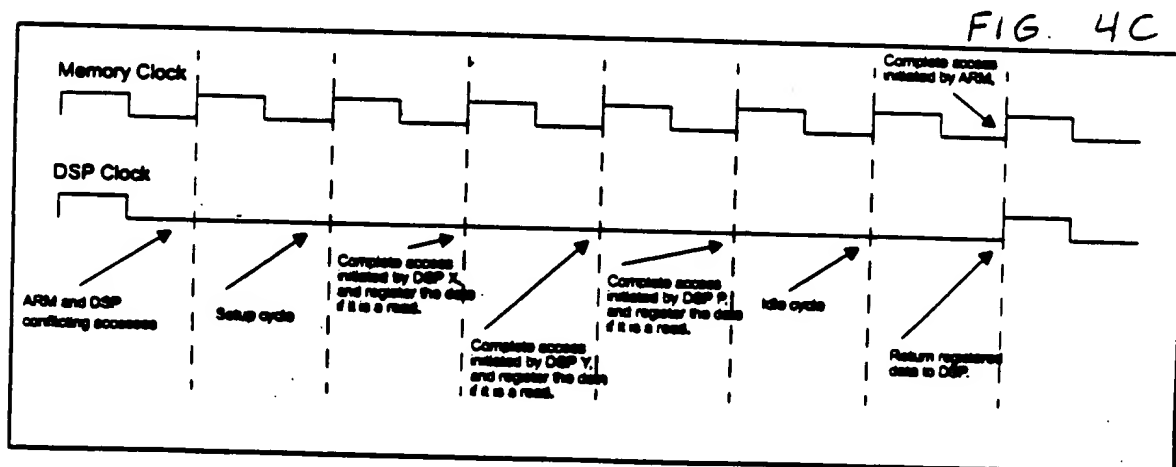
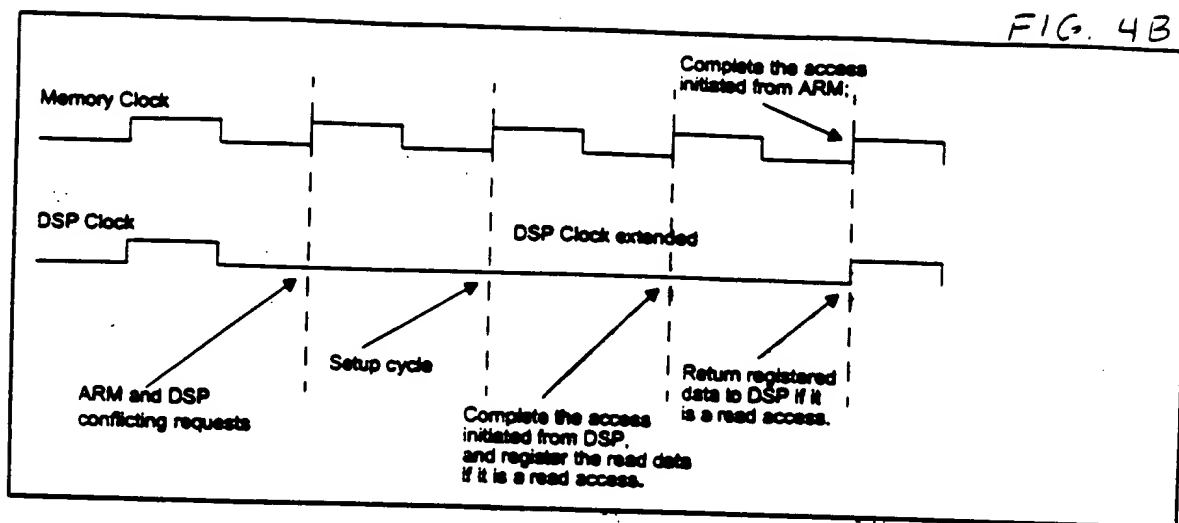
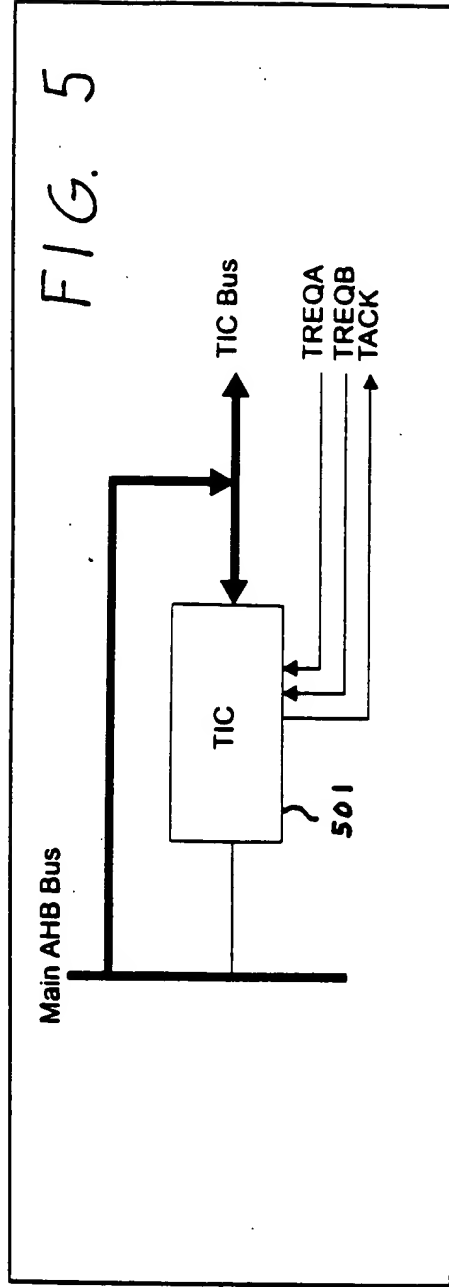
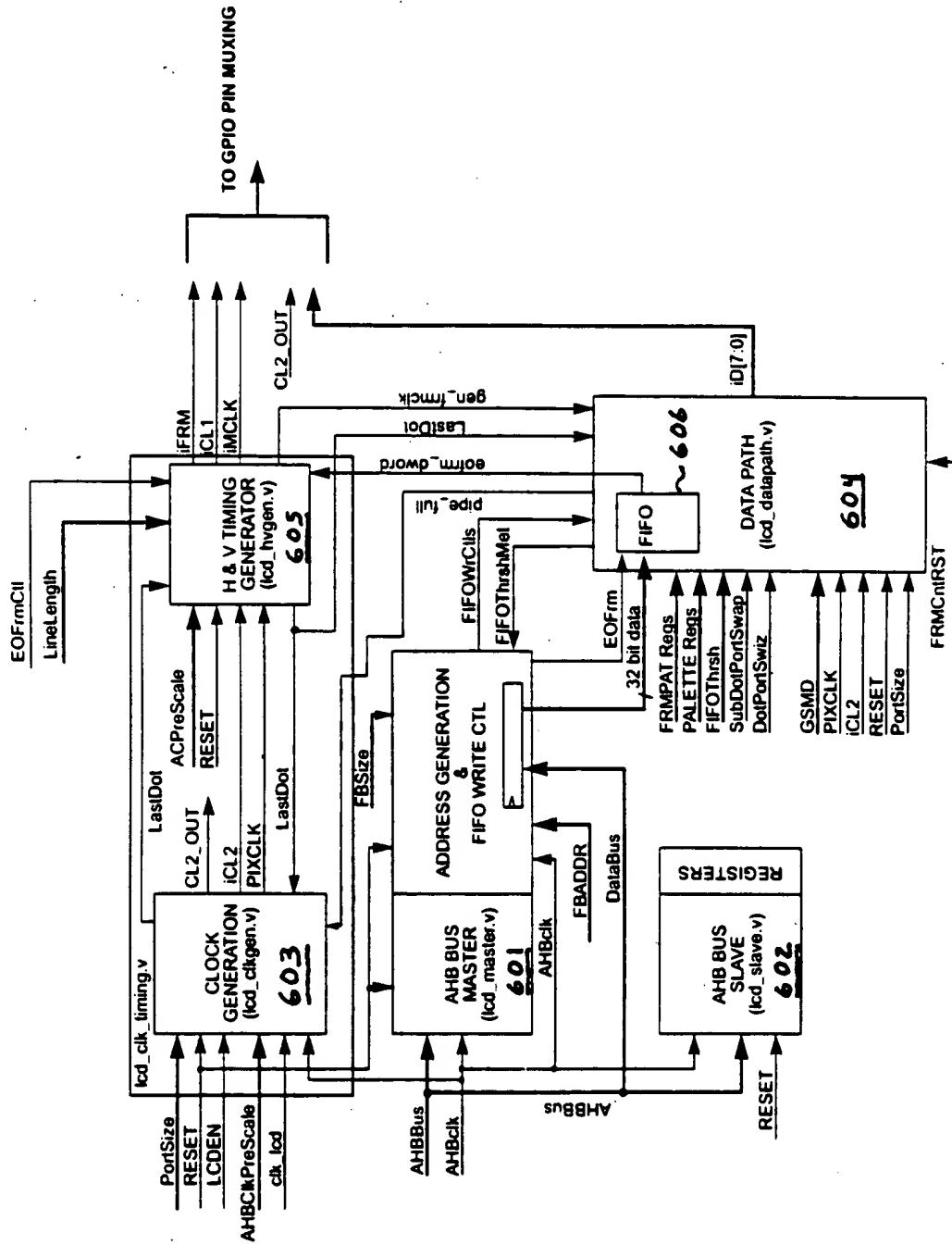


FIG. 4A







LCD Controller (lcd_top.v) Block Diagram

FIG. 6A

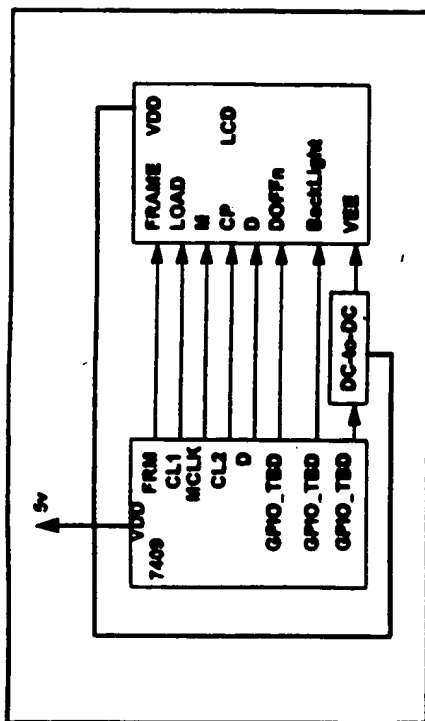


FIG 6B

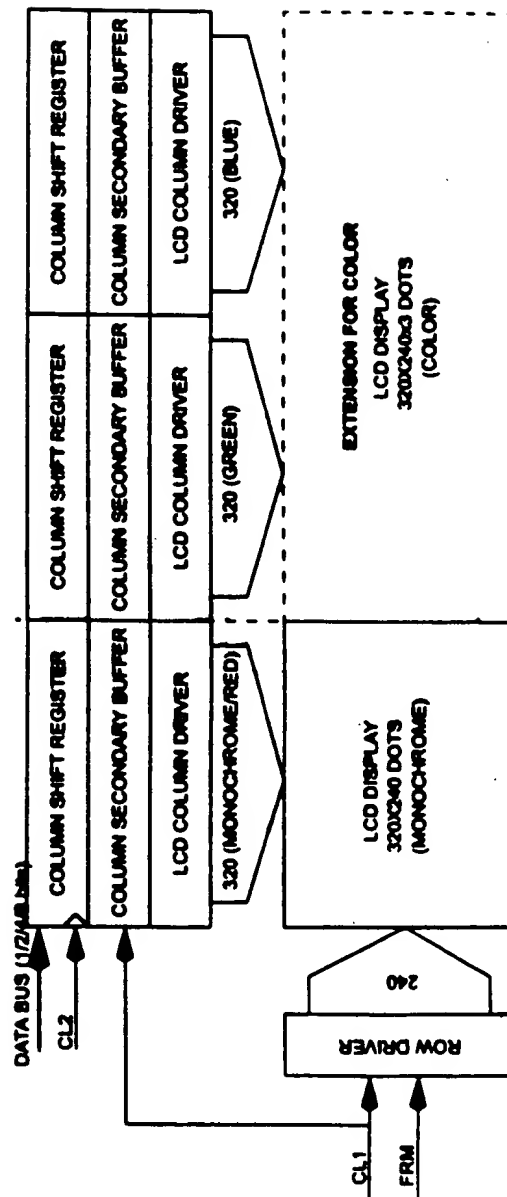


FIG. 6C

FIG 6 E

11

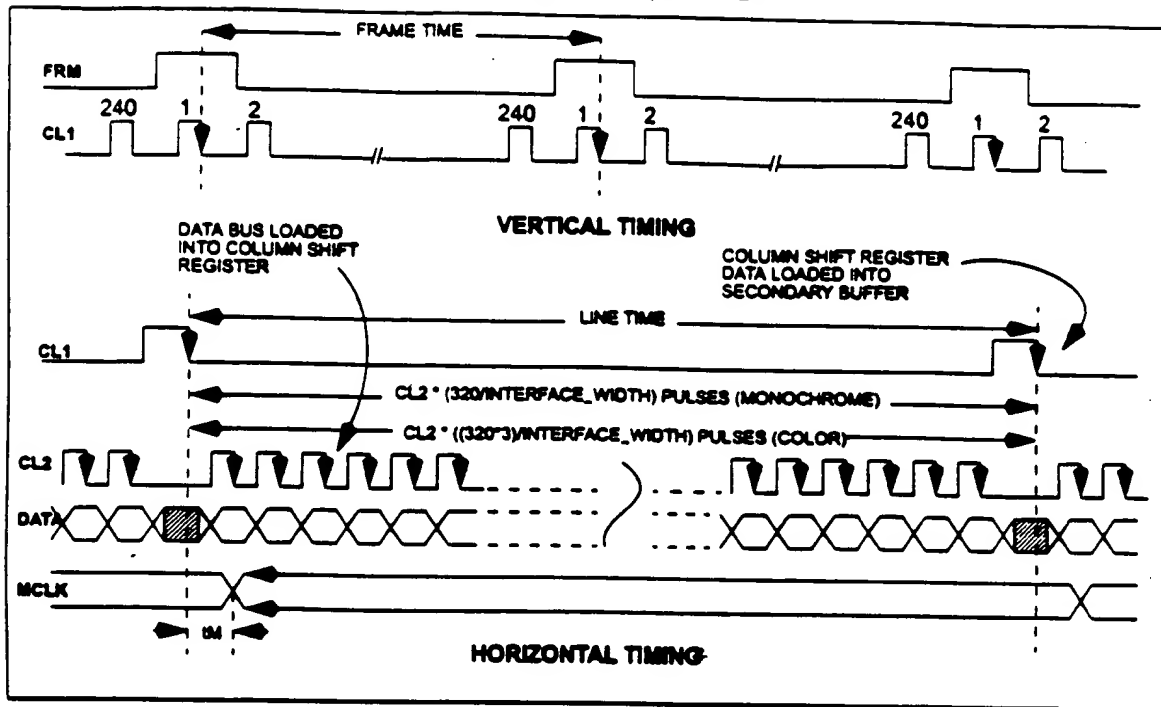


FIG 6 D

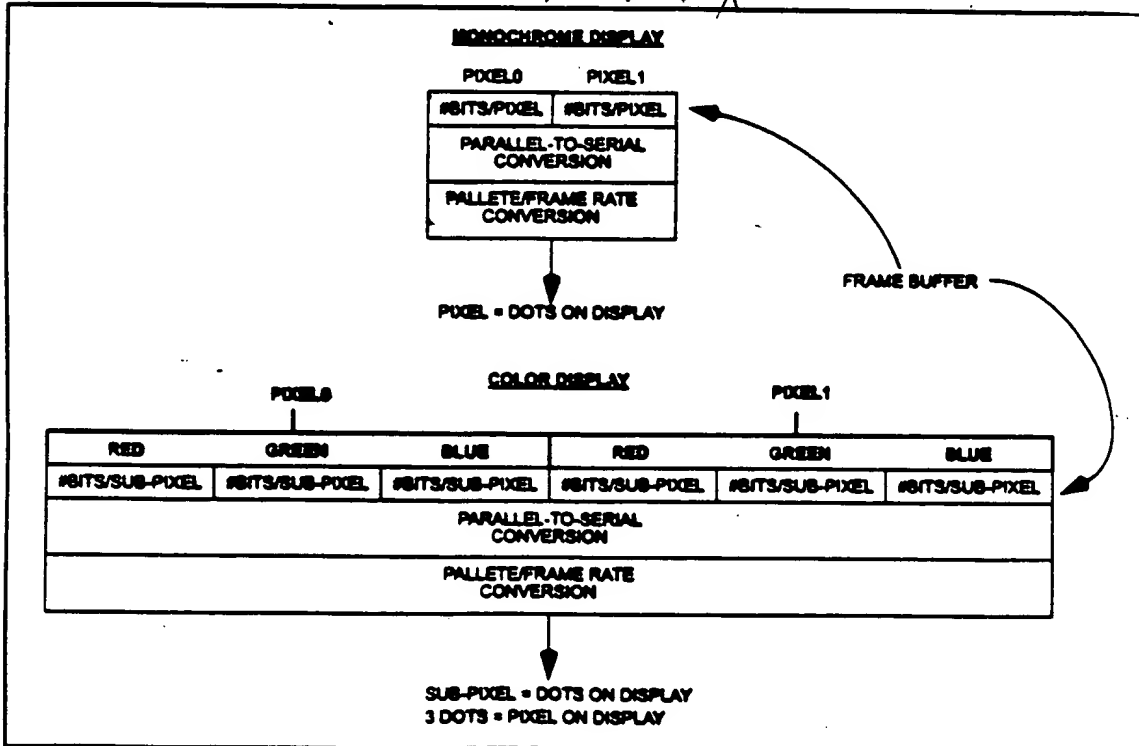


FIG. 6F

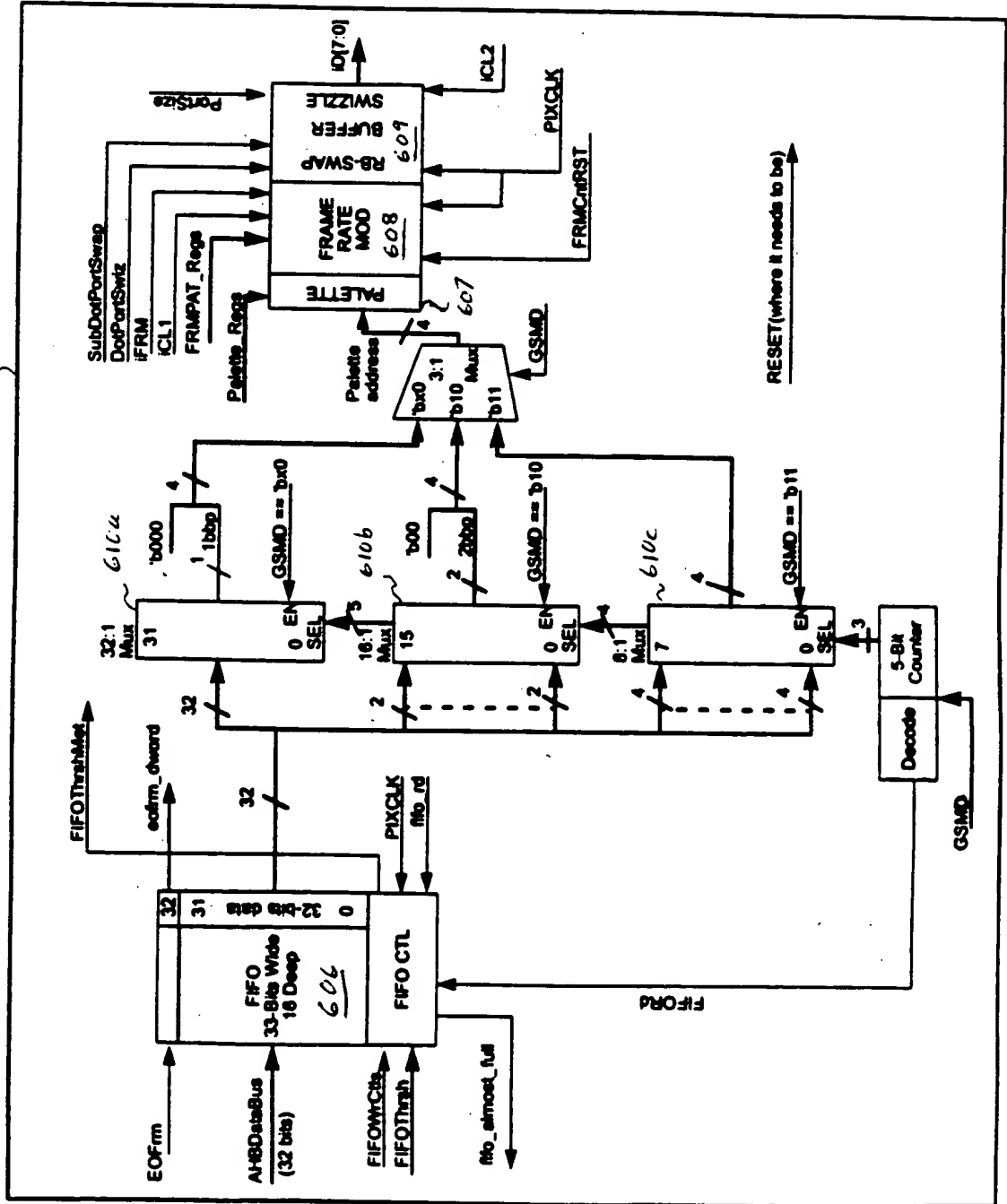


FIG 6G

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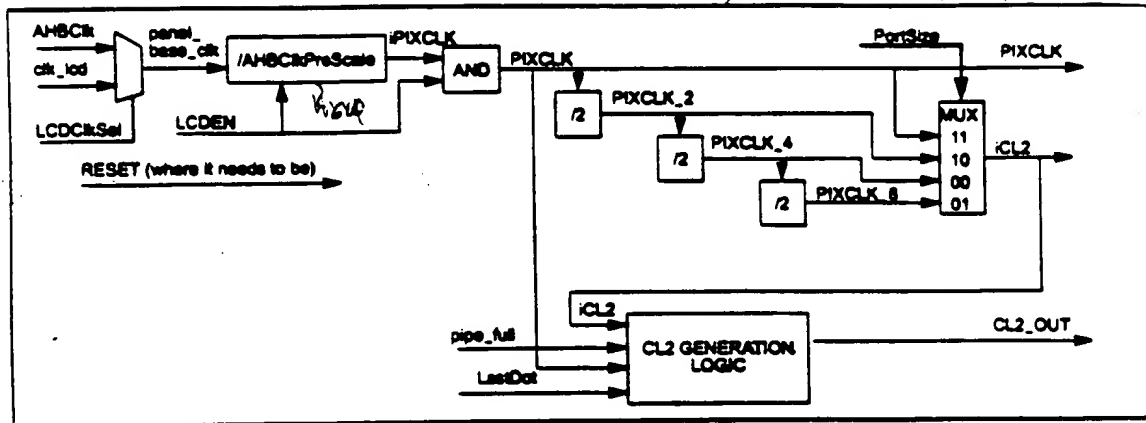


FIG 6H

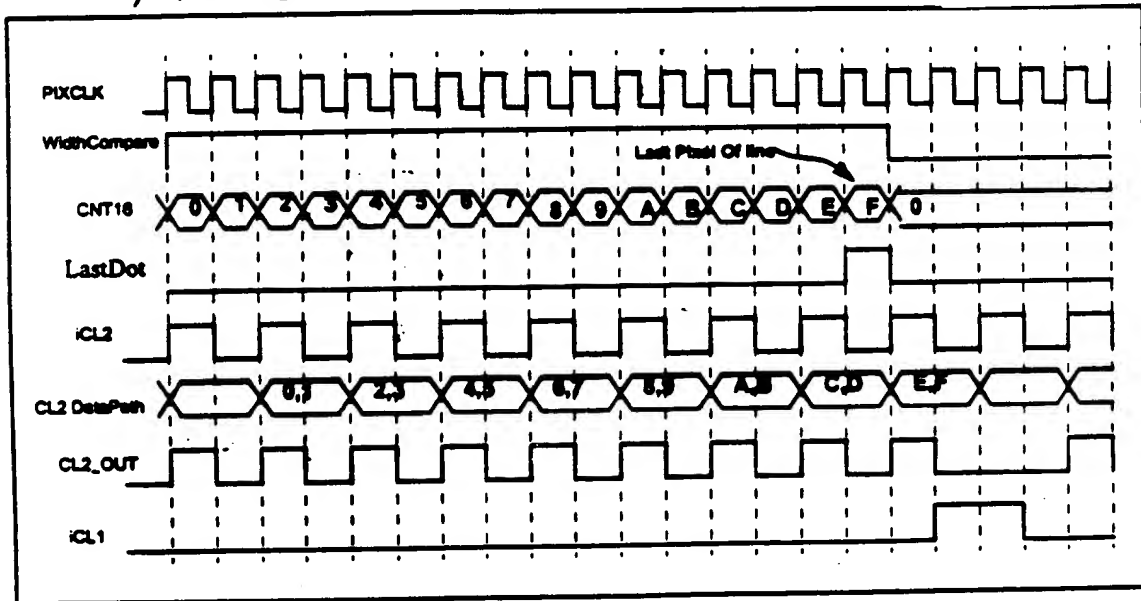


FIG 6 I 605

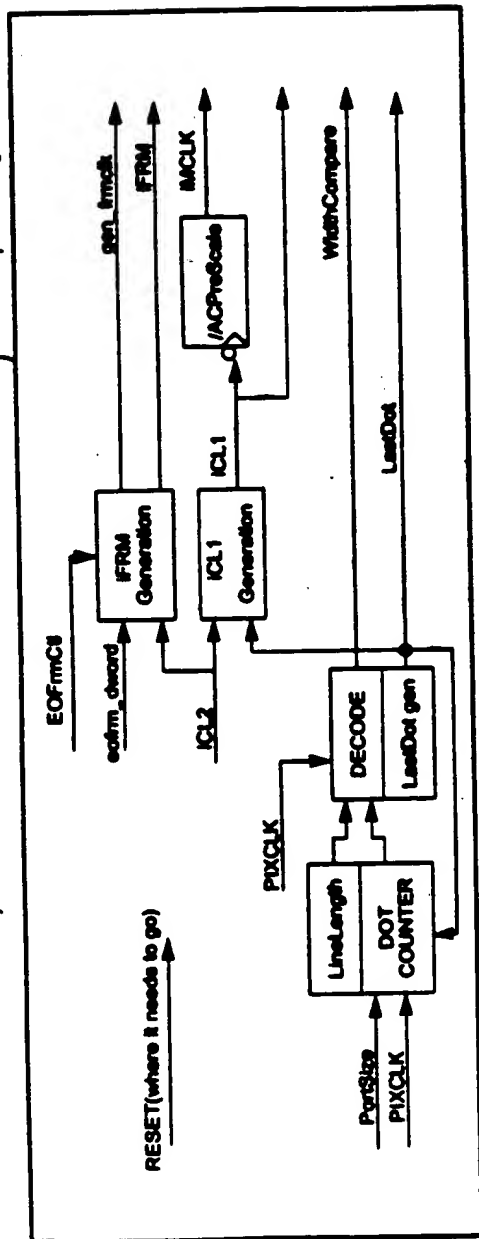


FIG 67

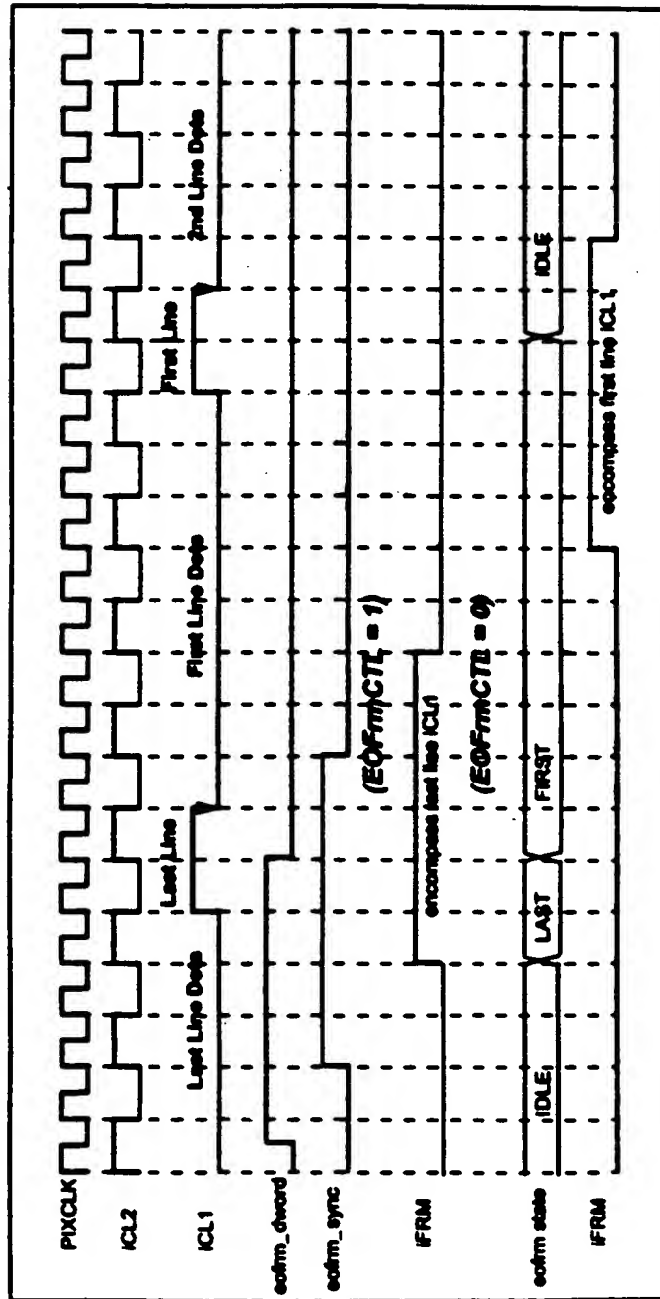


FIG. 6K

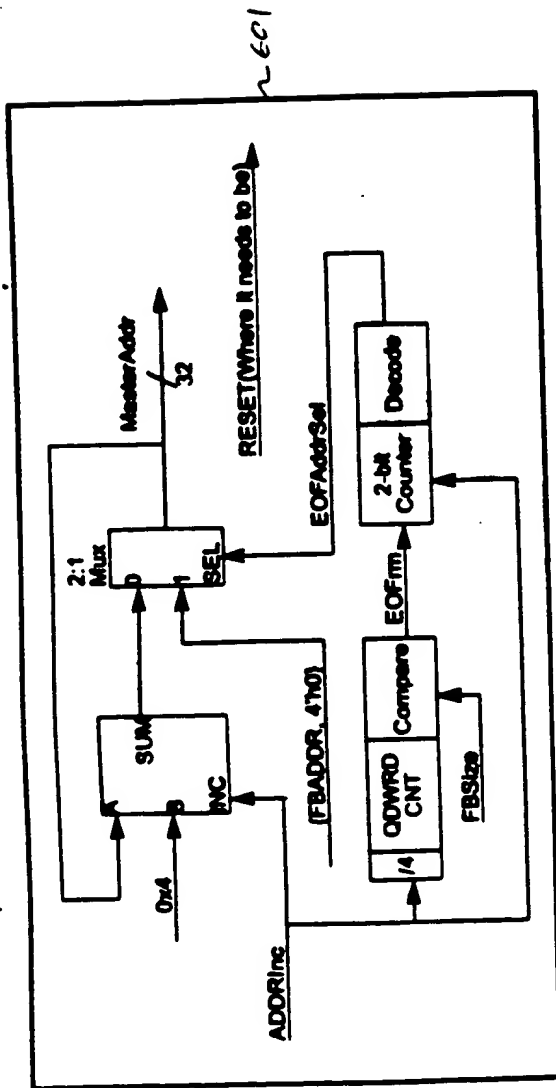


FIG 6L

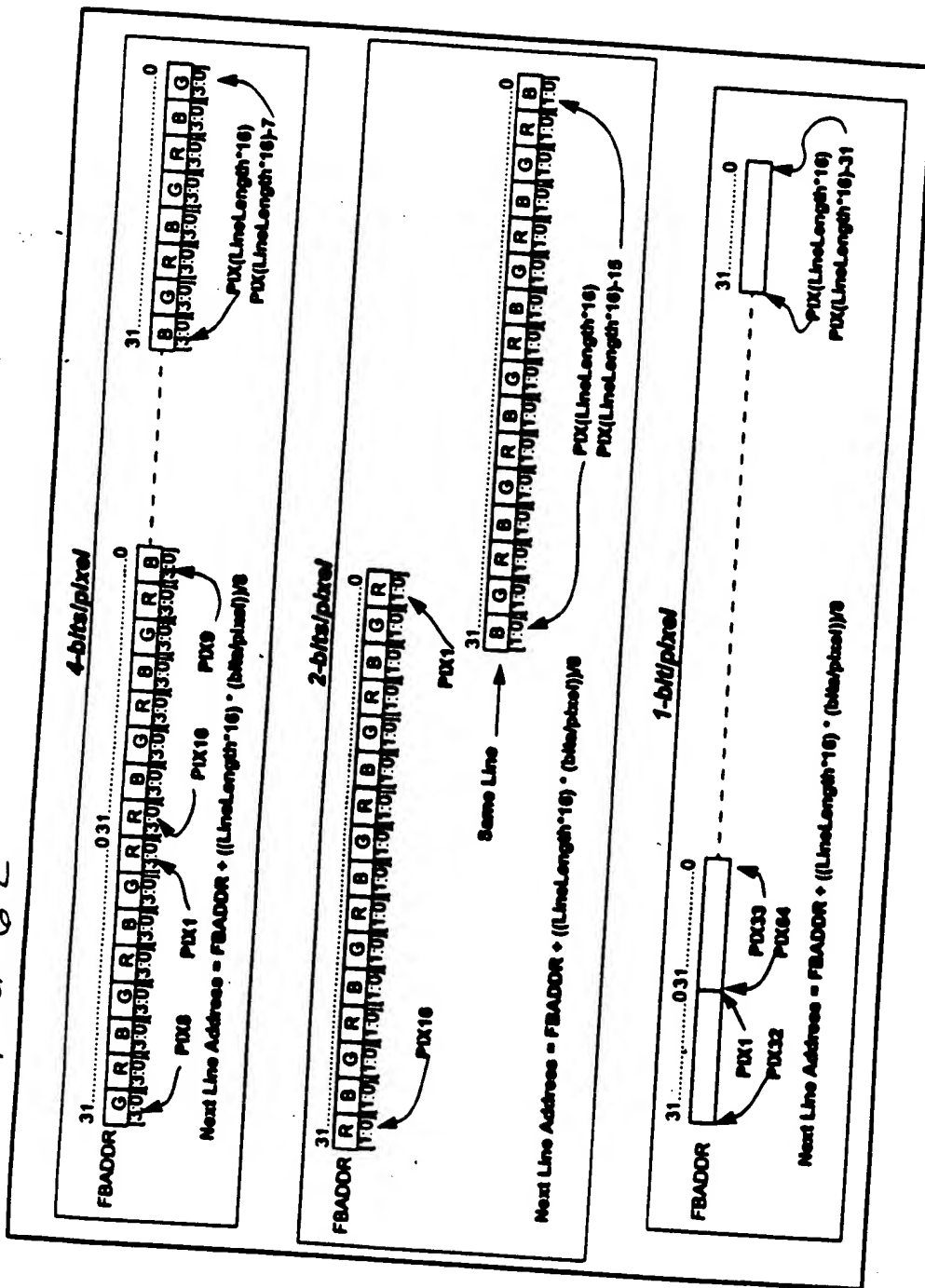


FIG 6M

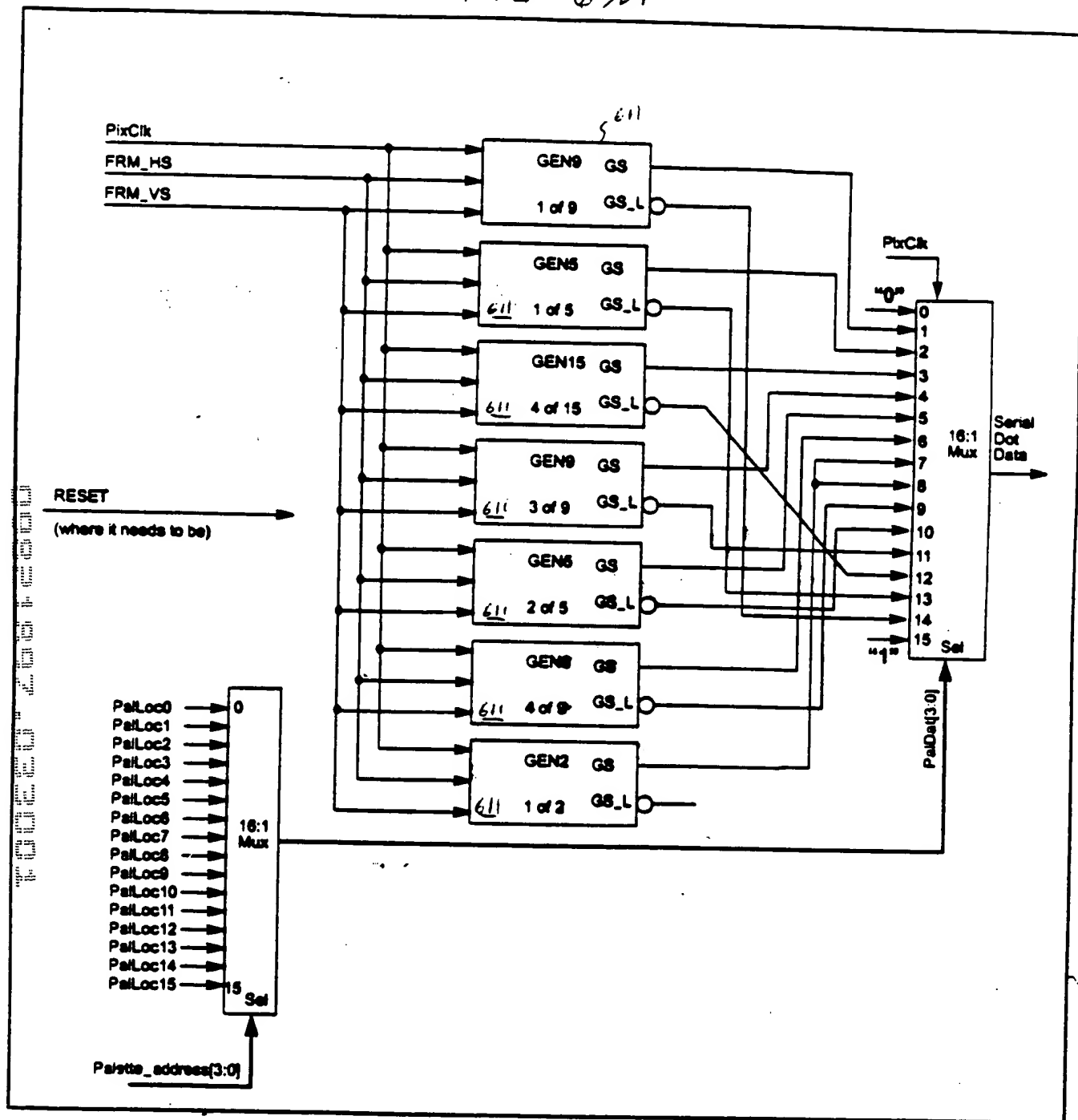
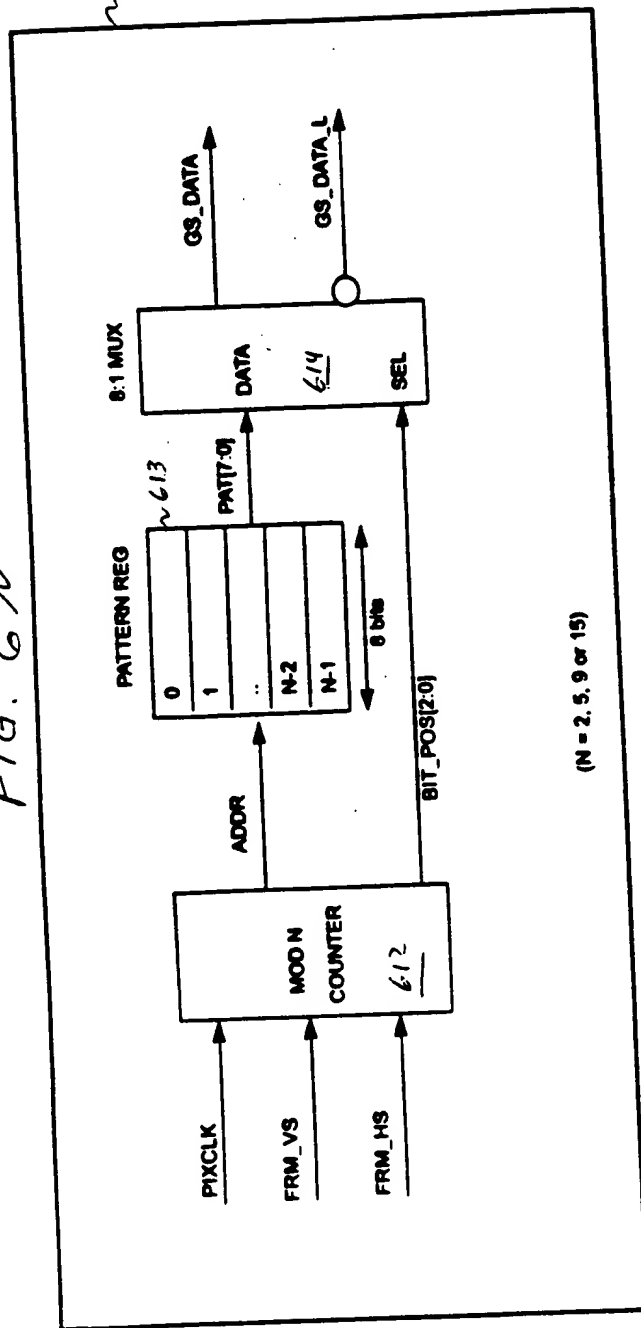


FIG. 6N



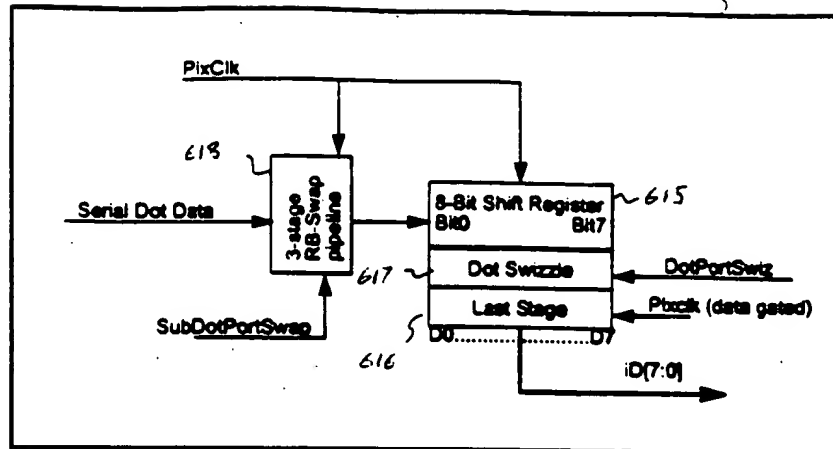


FIG 60

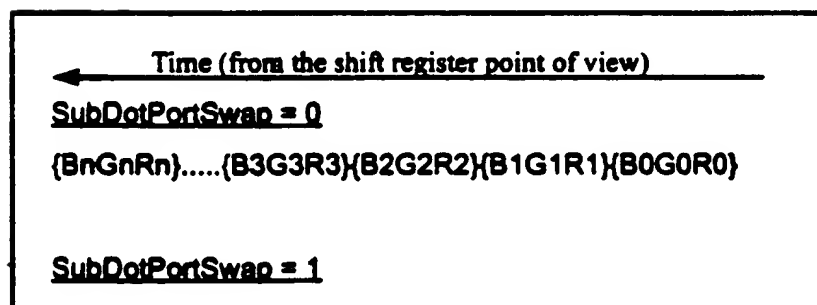


FIG. 6A

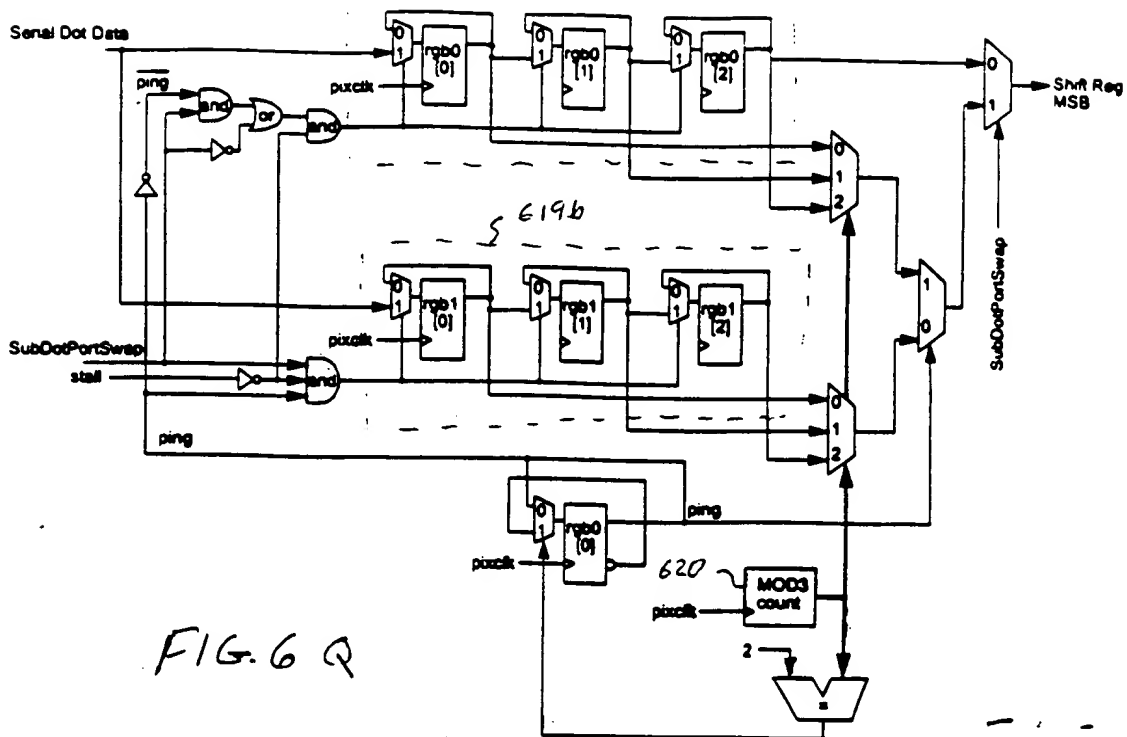


FIG 6.R

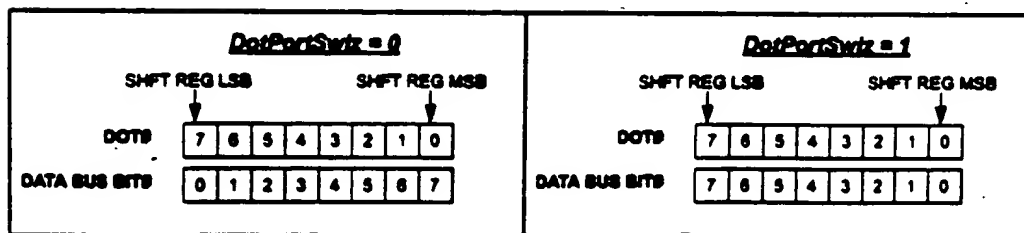
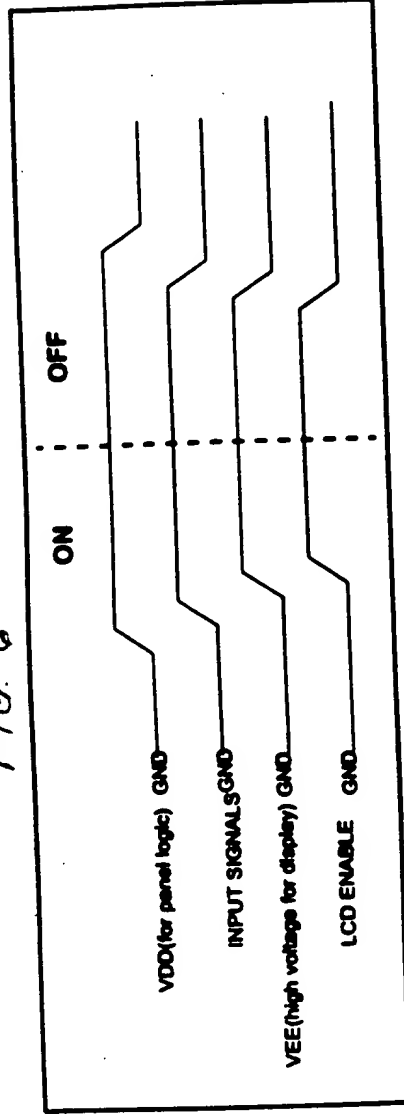


FIG. 6 S



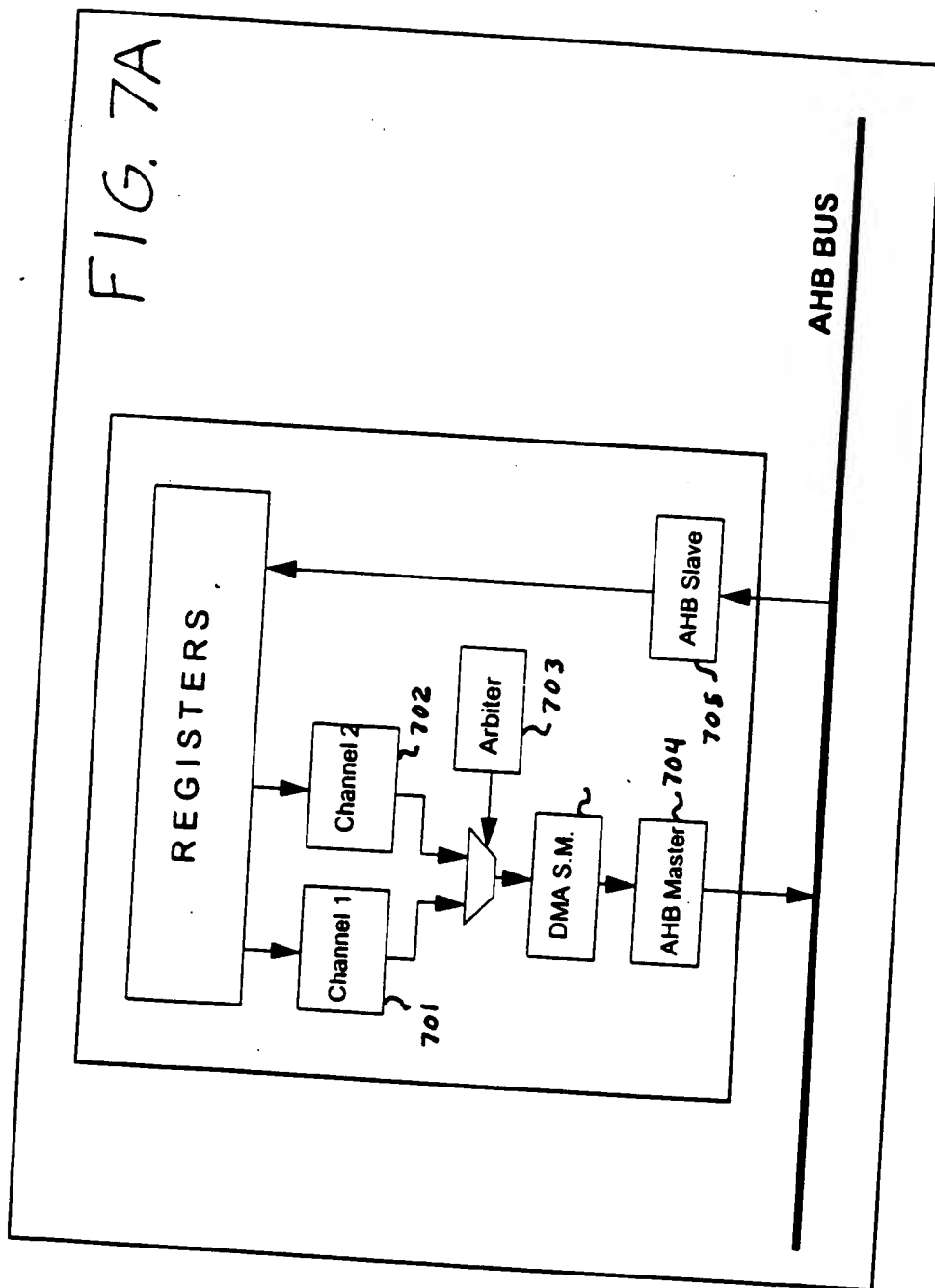


FIG. 7B

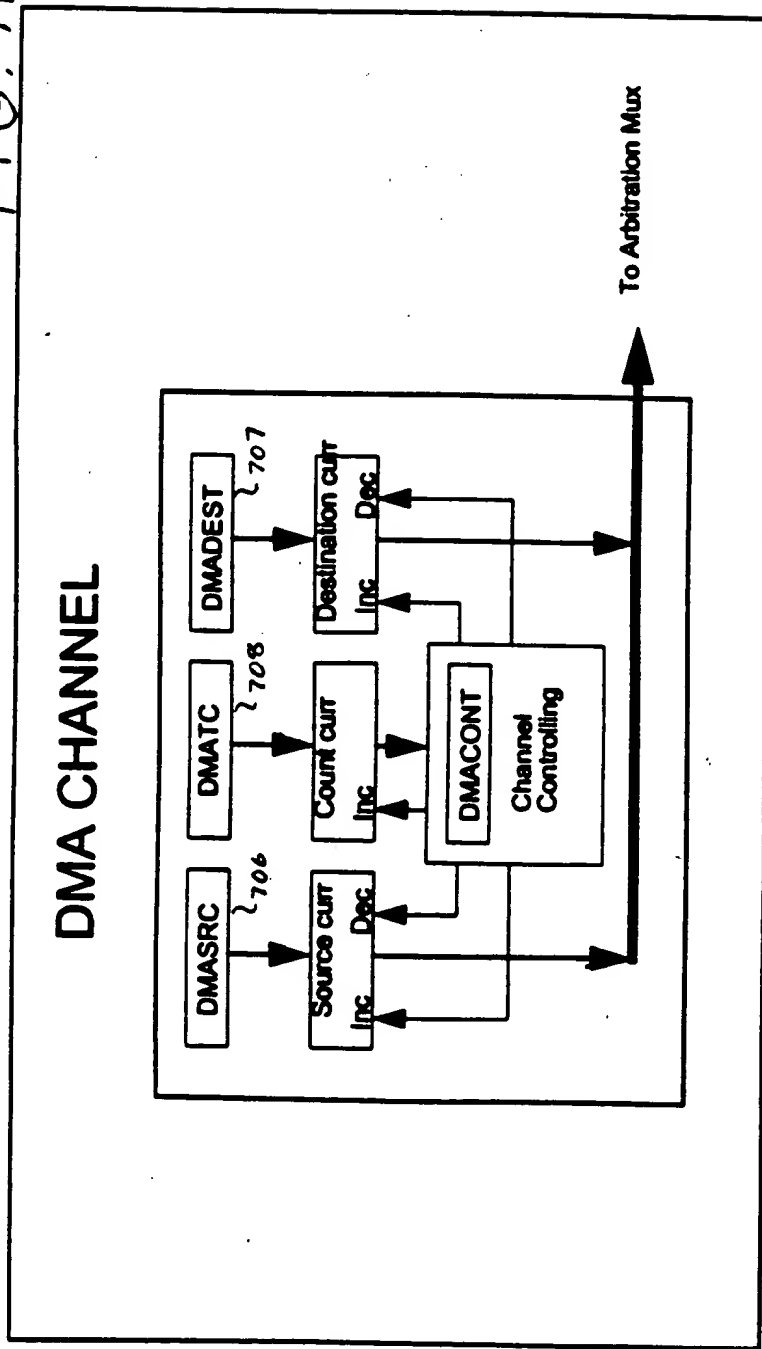
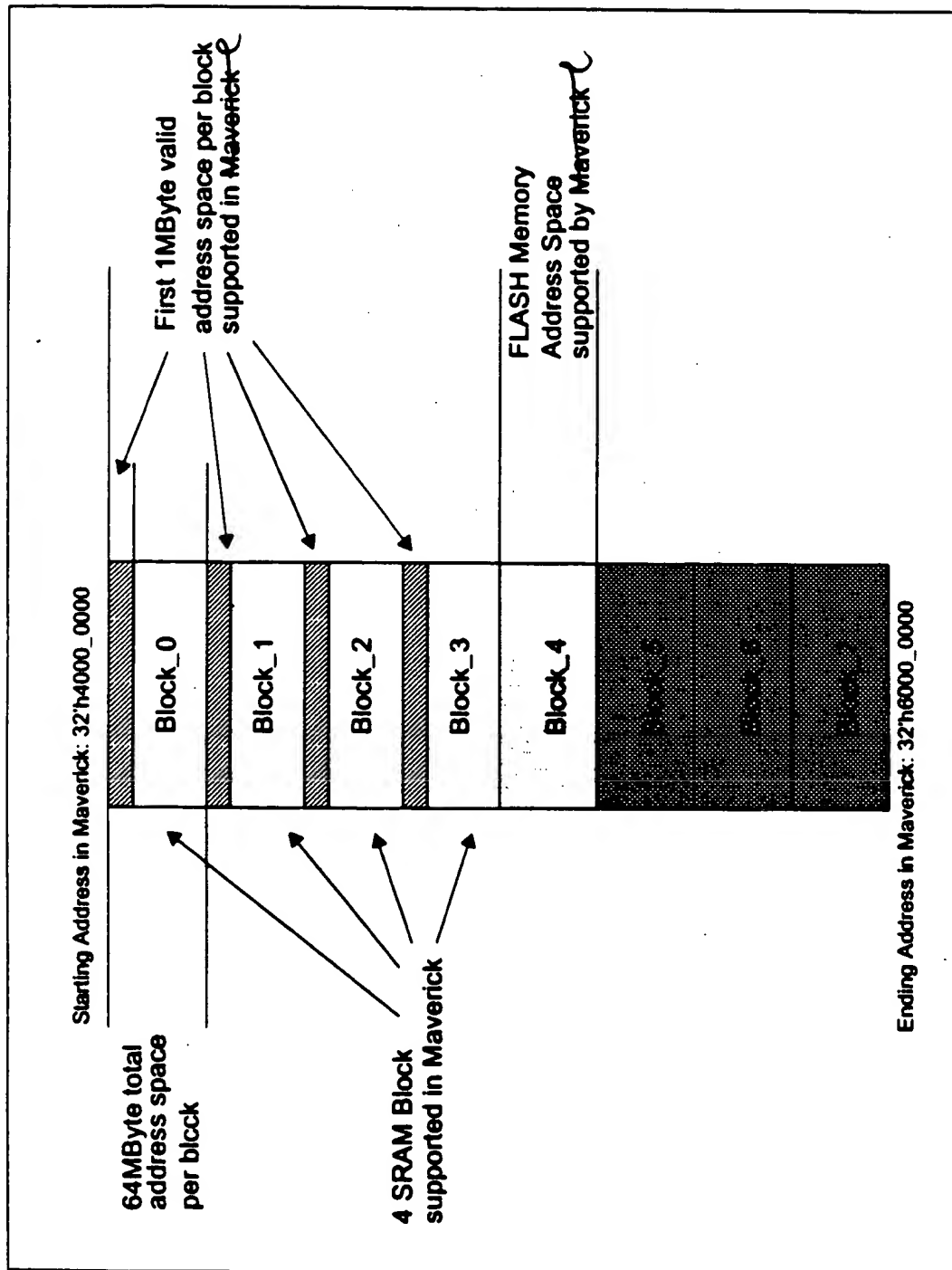
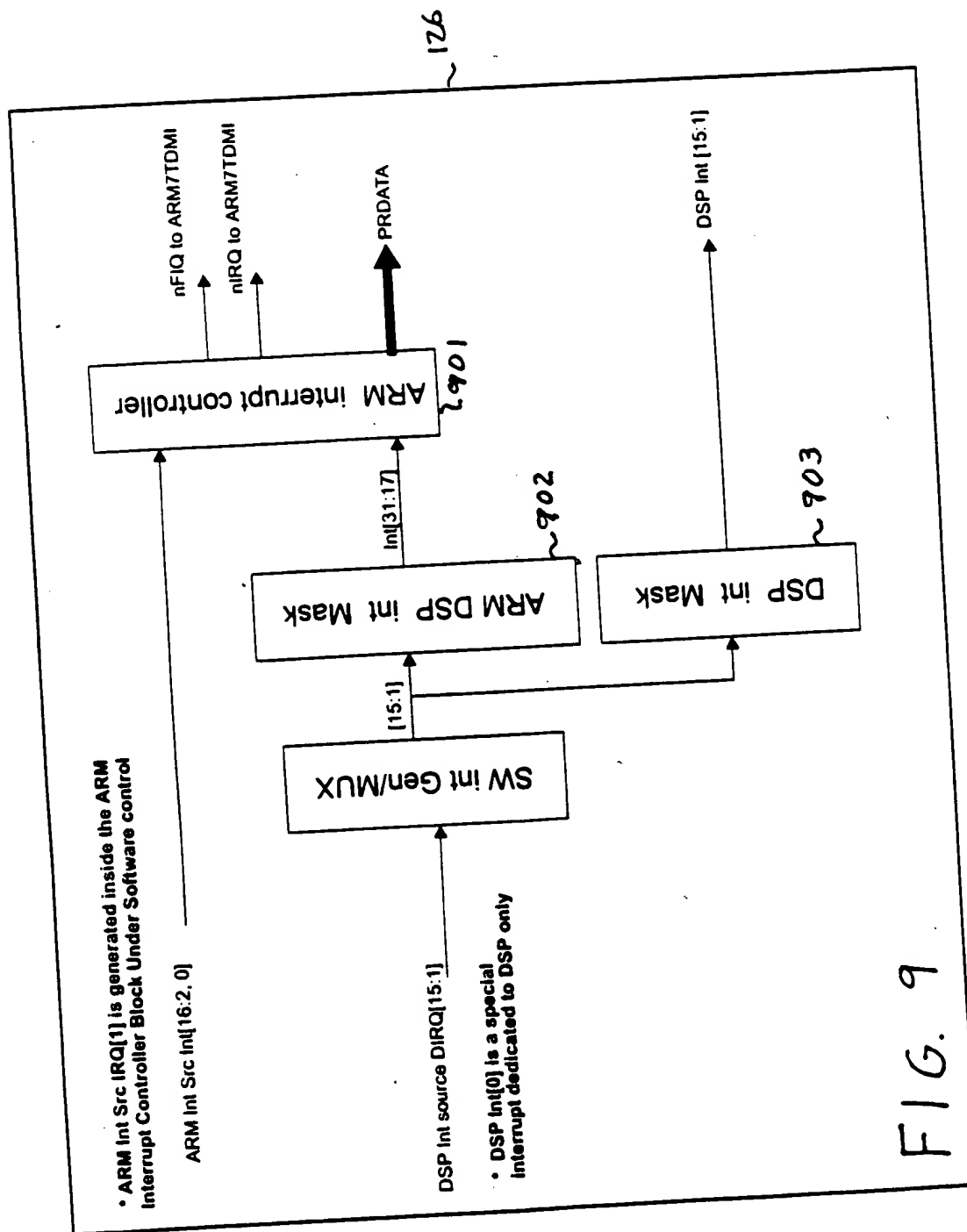


FIG. 8





• ARM int Src IRQ[1] is generated inside the ARM Interrupt Controller Block Under Software control

• DSP int[0] is a special interrupt dedicated to DSP only

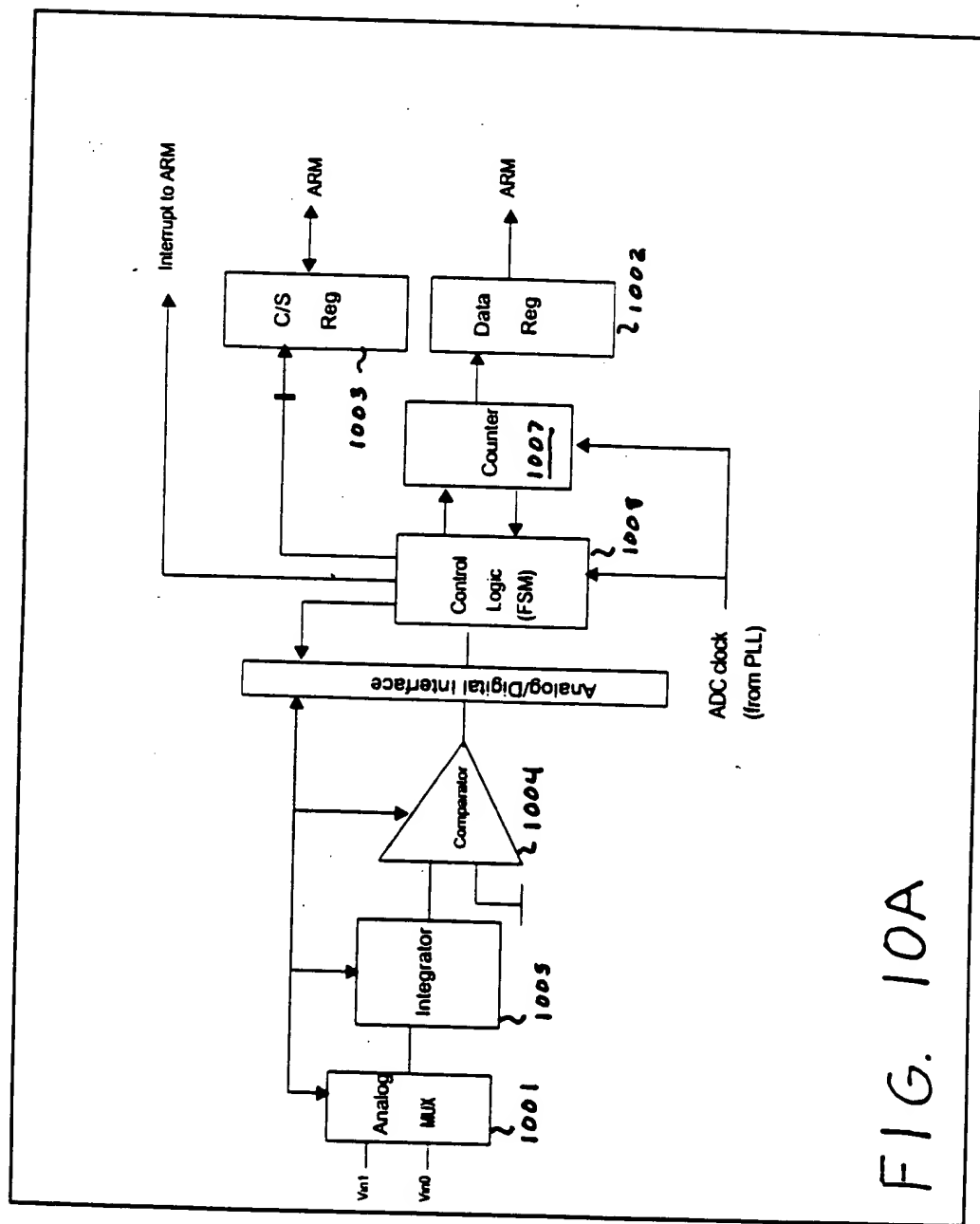


FIG. 10A

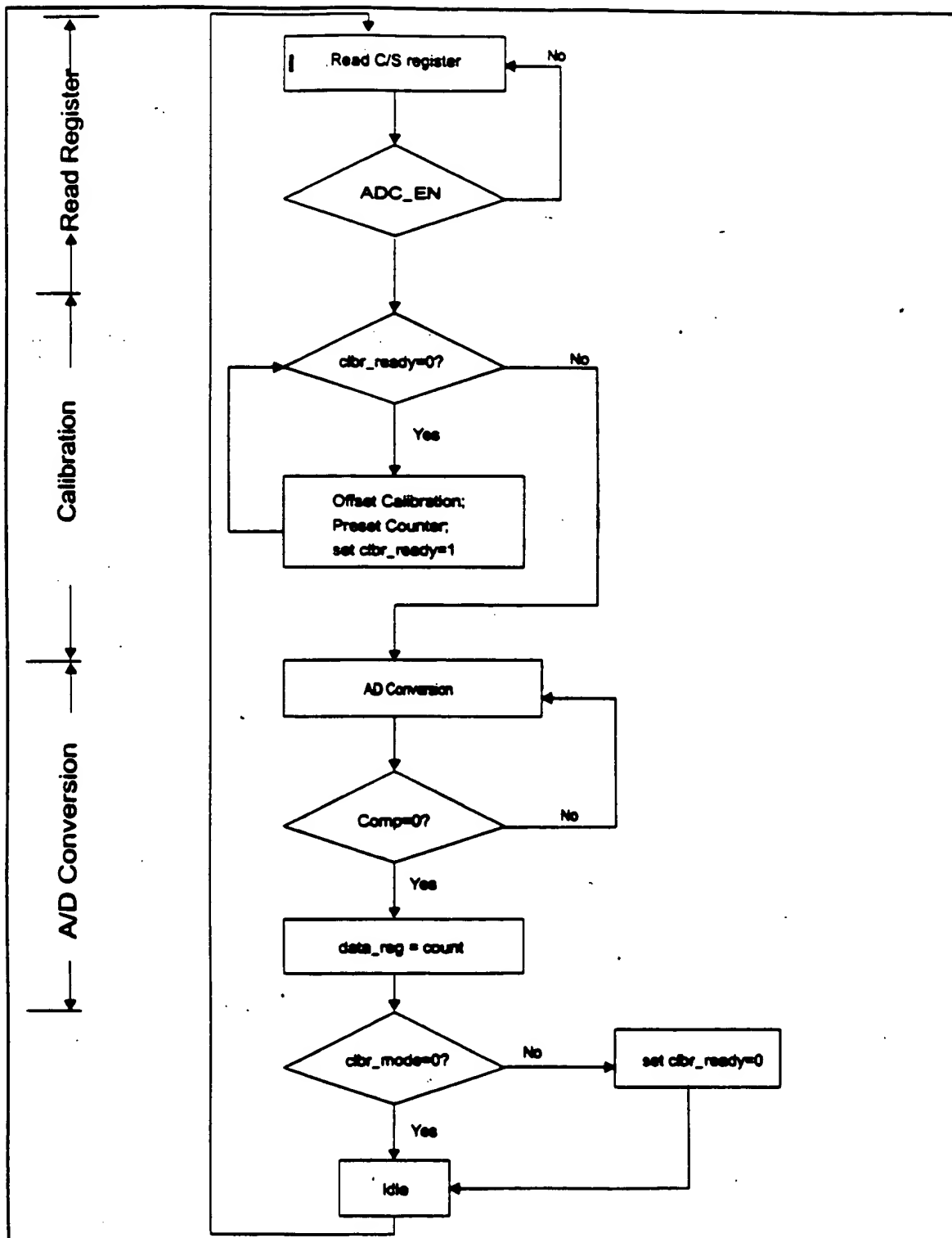
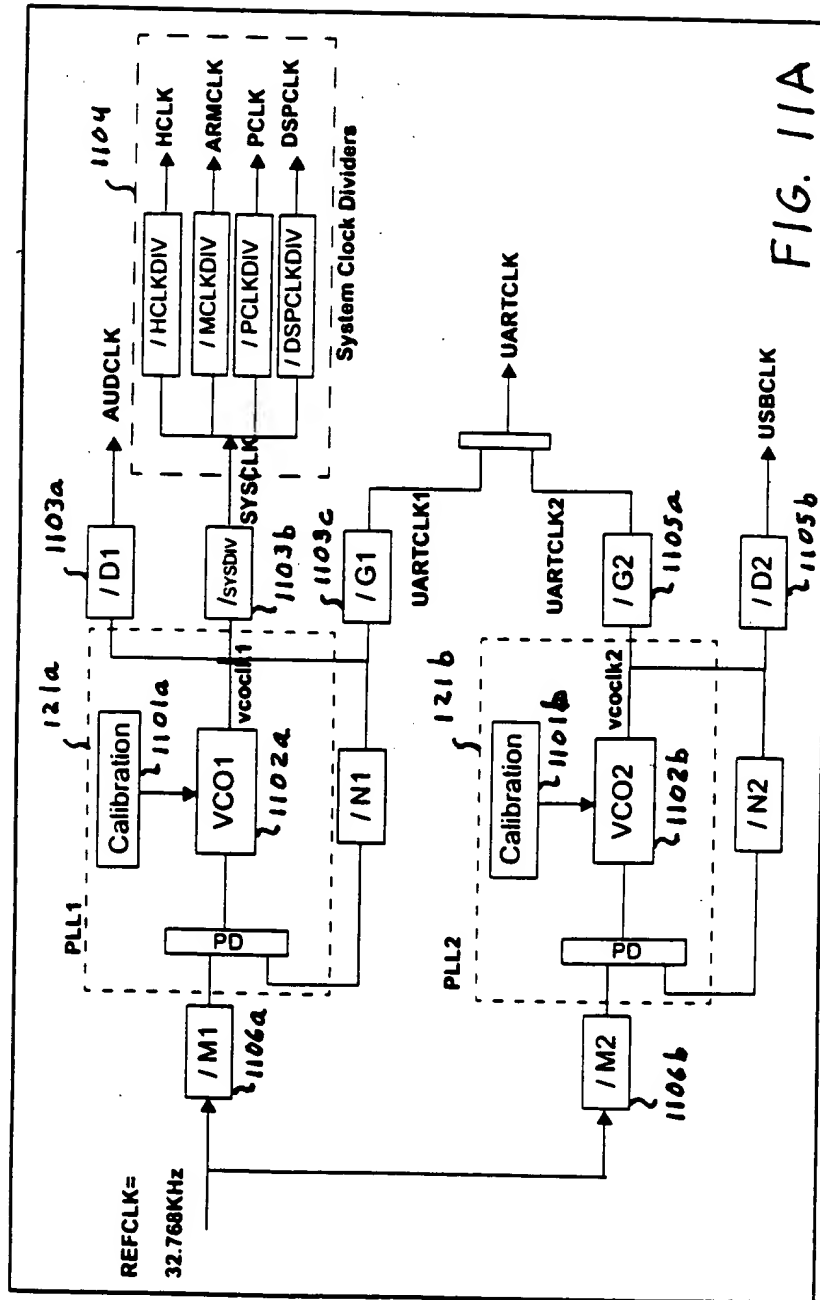


FIG. 10B

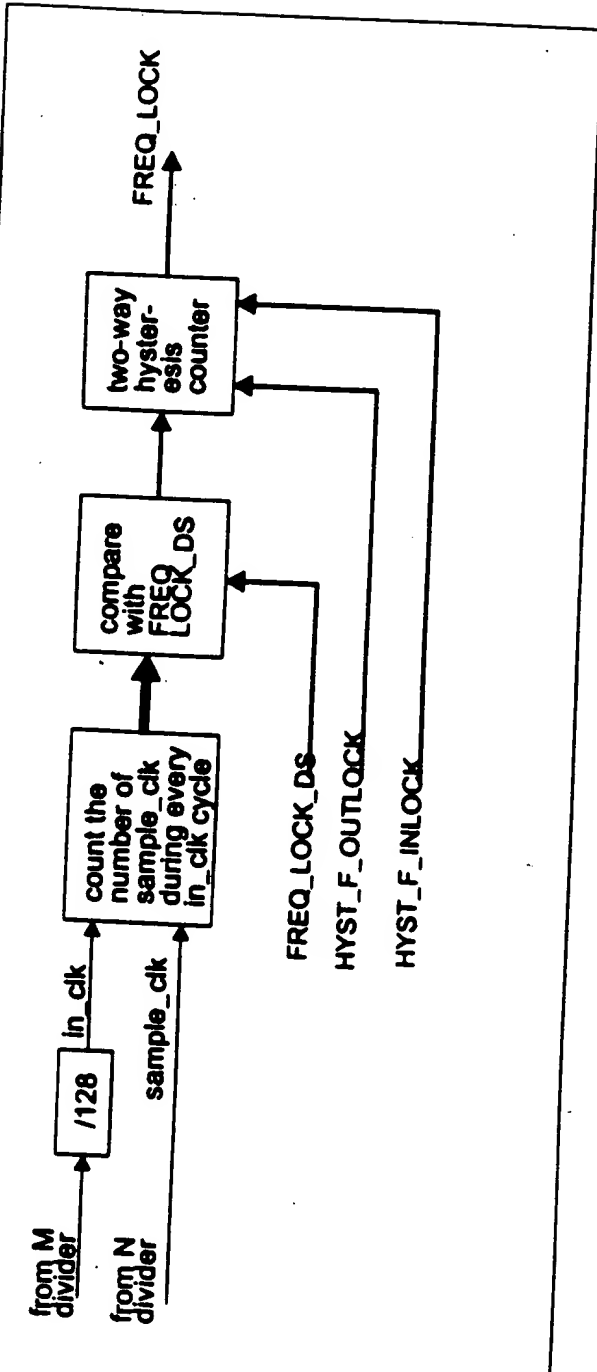


The diagram illustrates a dual PLL system for a microcontroller. It features two PLLs, PLL1 (top) and PLL2 (bottom), each with a VCO, Freq/Phase lock det, and various dividers. PLL1 outputs include VB_LOCK1, DSPBY, USBBY, AUDCLK, HCLK, ARMCLK, PCLK, DSPCLK, lockb1, UARTCLK, lockb2, LCDCLK, and USBCLK. PLL2 outputs include VB_LOCK2. The diagram is annotated with handwritten labels like 1109a, 1110a, 1105a, 1107a, 1107b, 1106b, 1109b, and 1105b.

FIG. 11C

```
graph LR; A[up_dn_diff from PD] --> B[Count during low pulse]; C[clock from vco] --> B; B --> D[compare with PHASE_LOCK_DS]; D --> E[PHASE_LOCK];
```


FIG. 11D



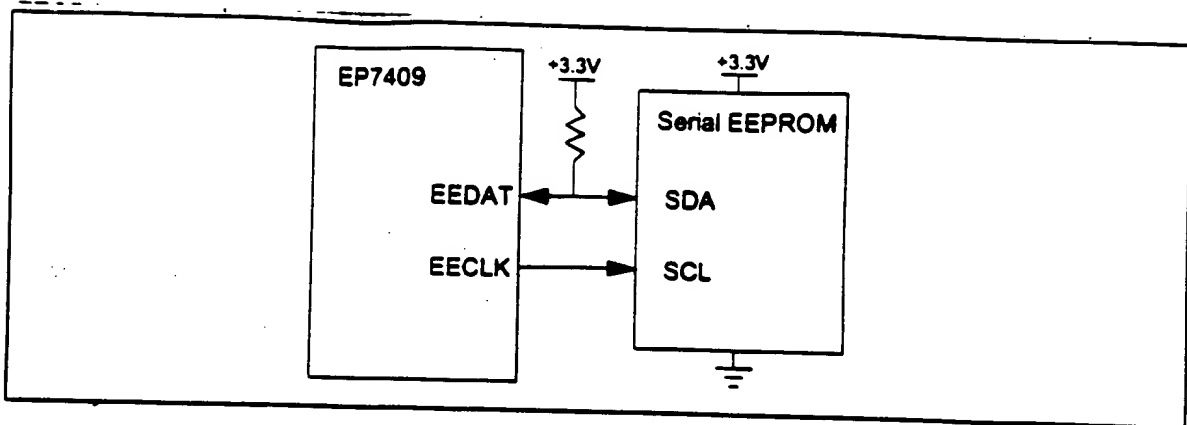


Fig. 12 A

Fig 12 B

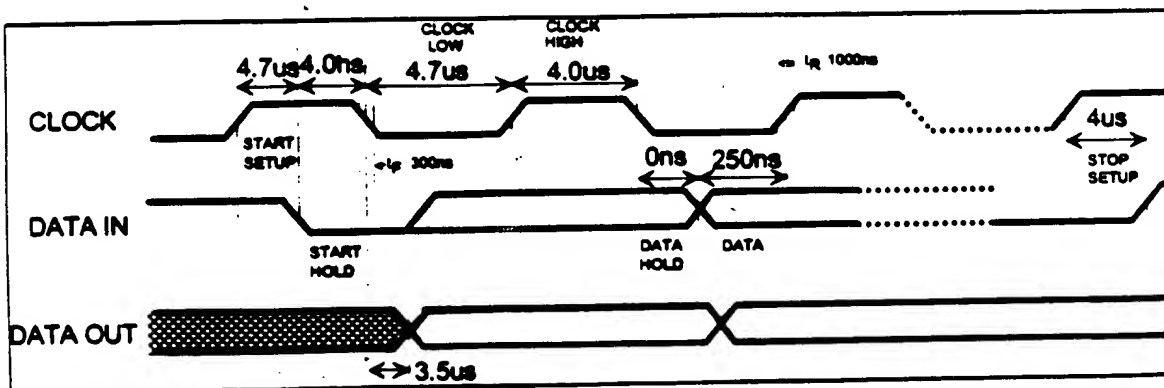
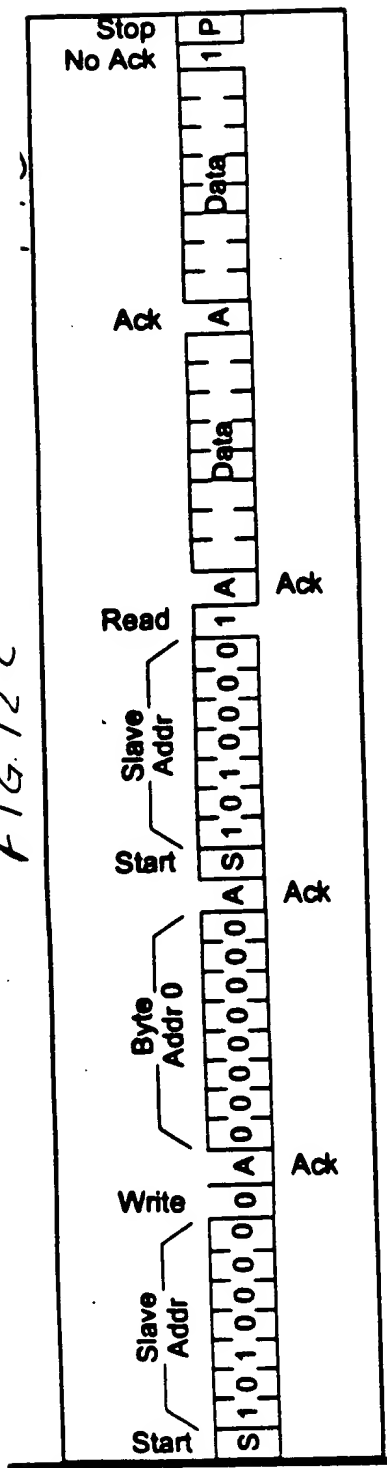


FIG. 12c



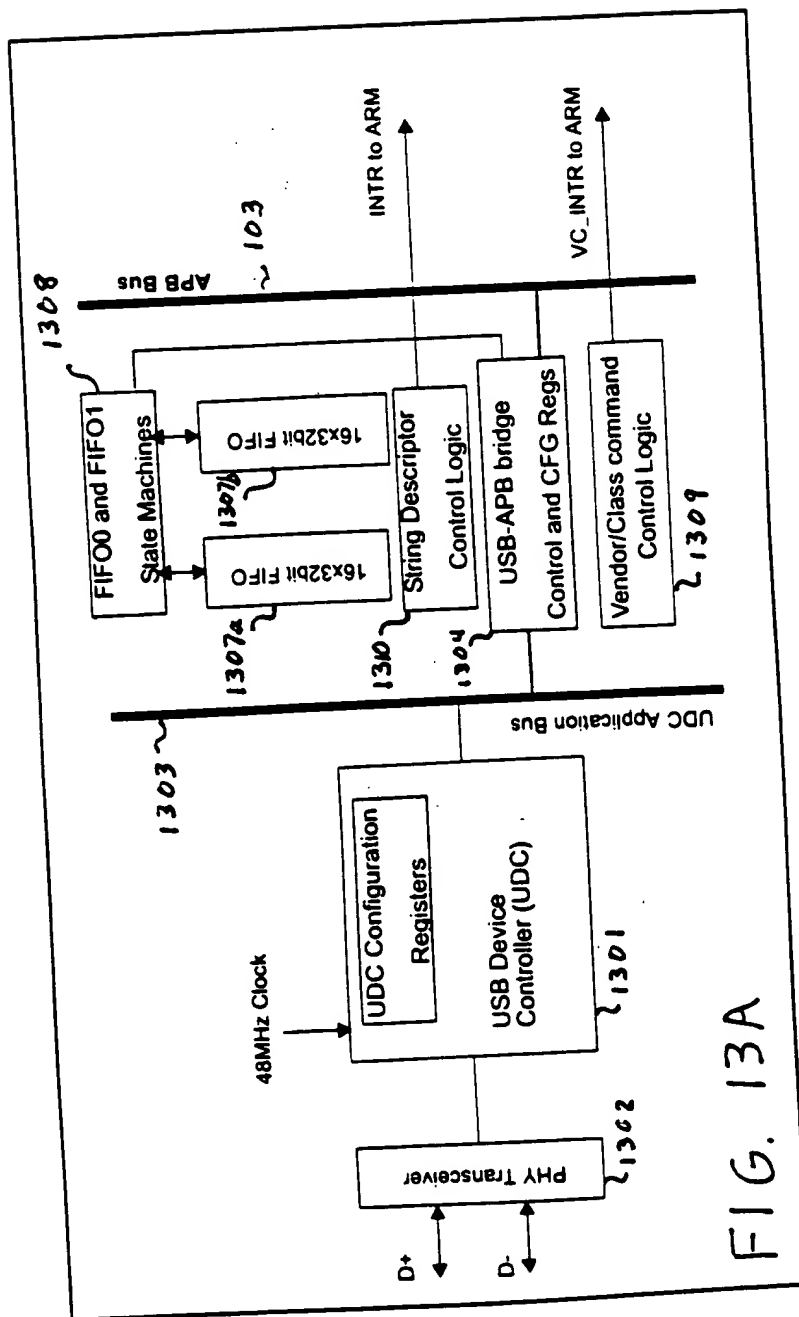


FIG. 13B

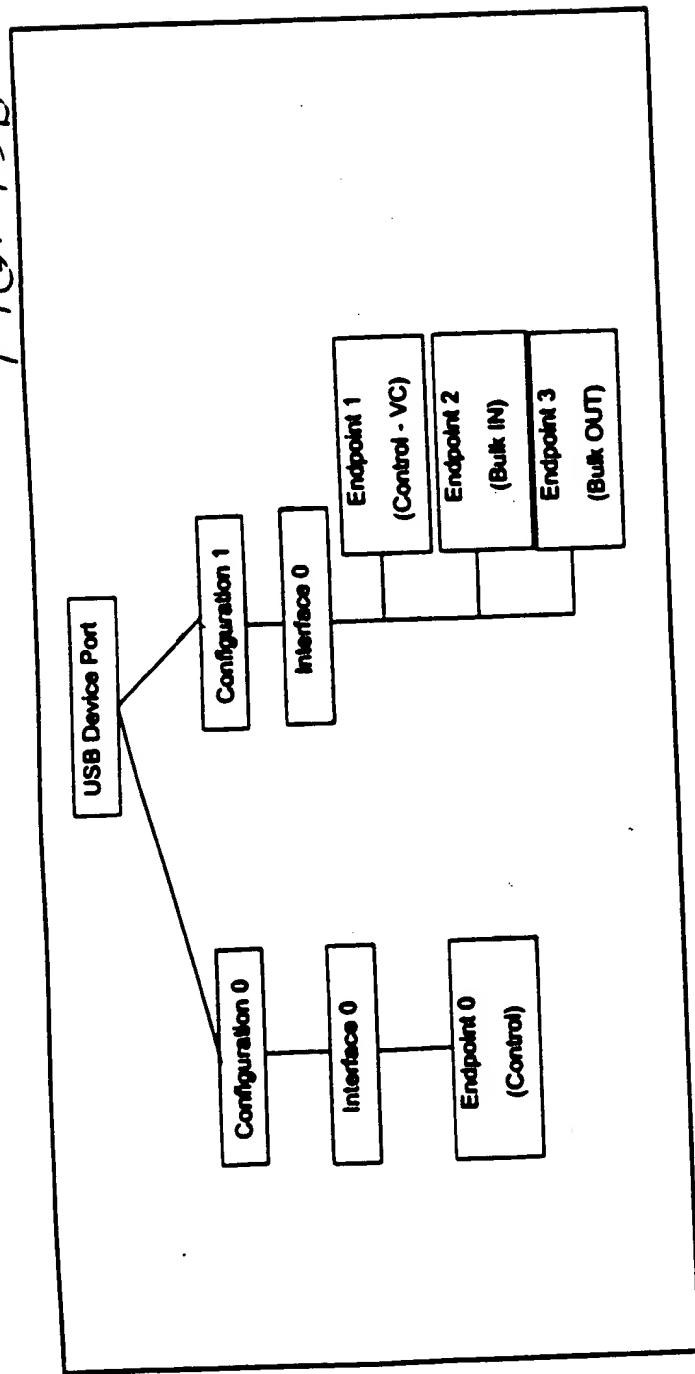


FIG. 14

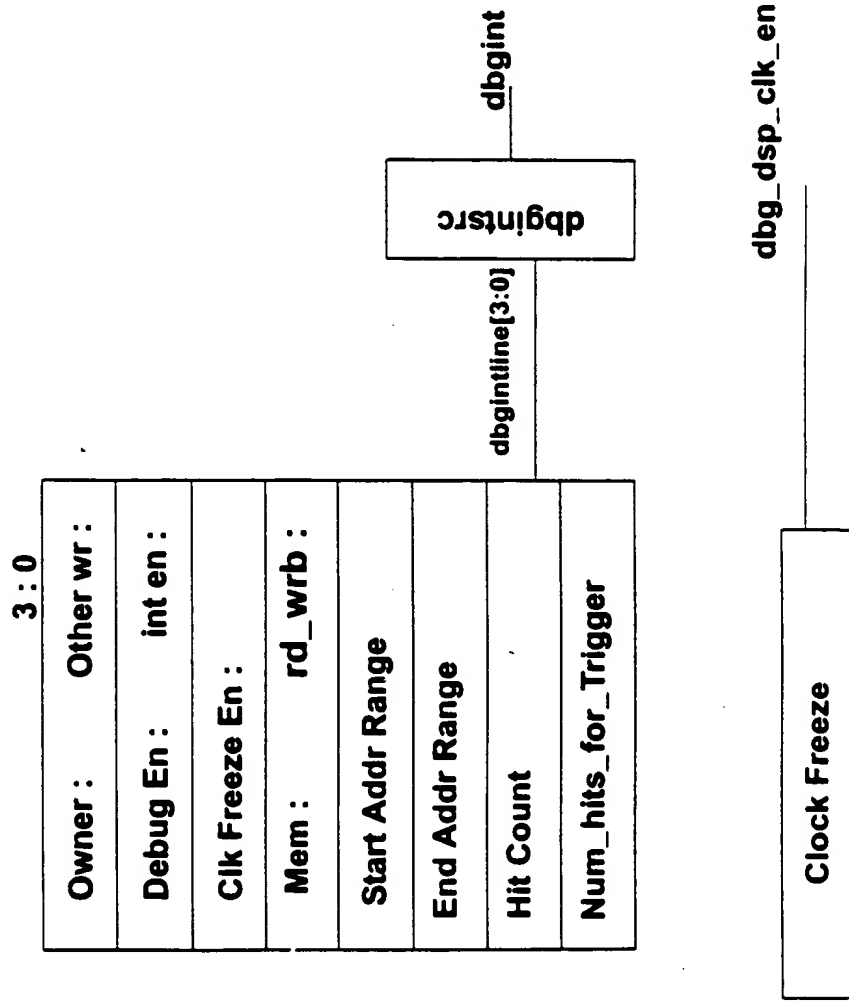
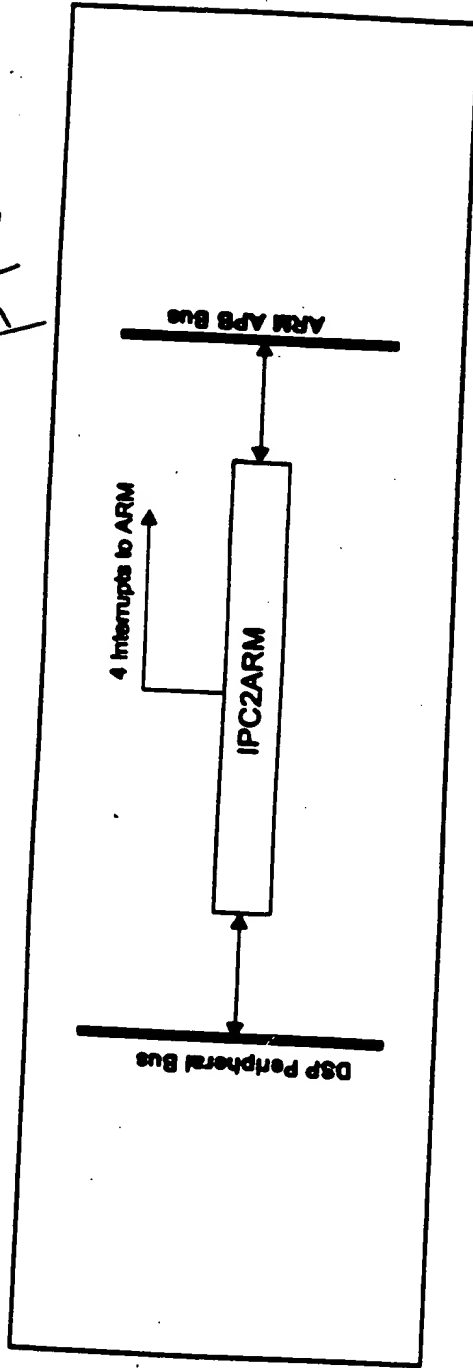


FIG. 15



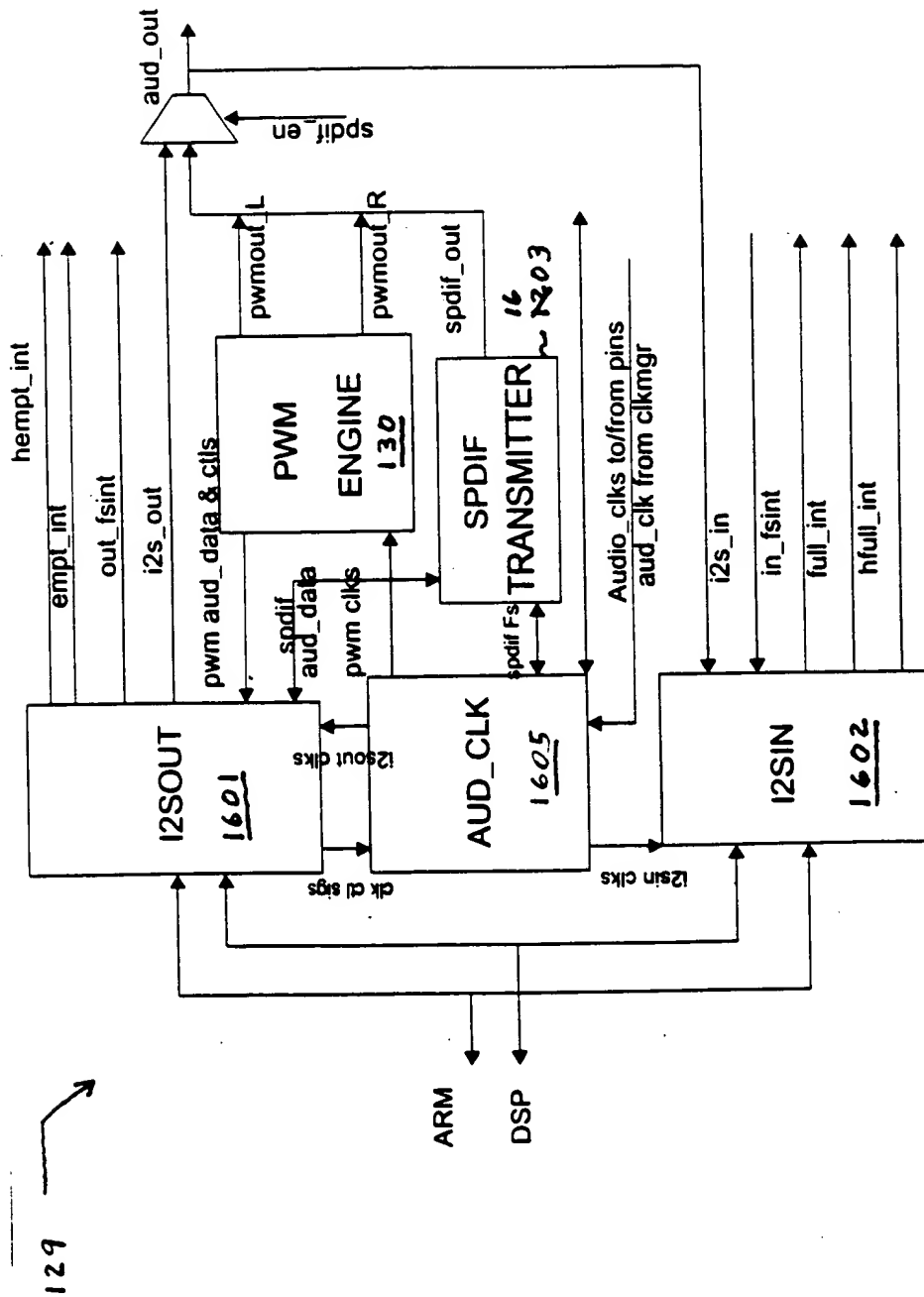


FIG. 16A

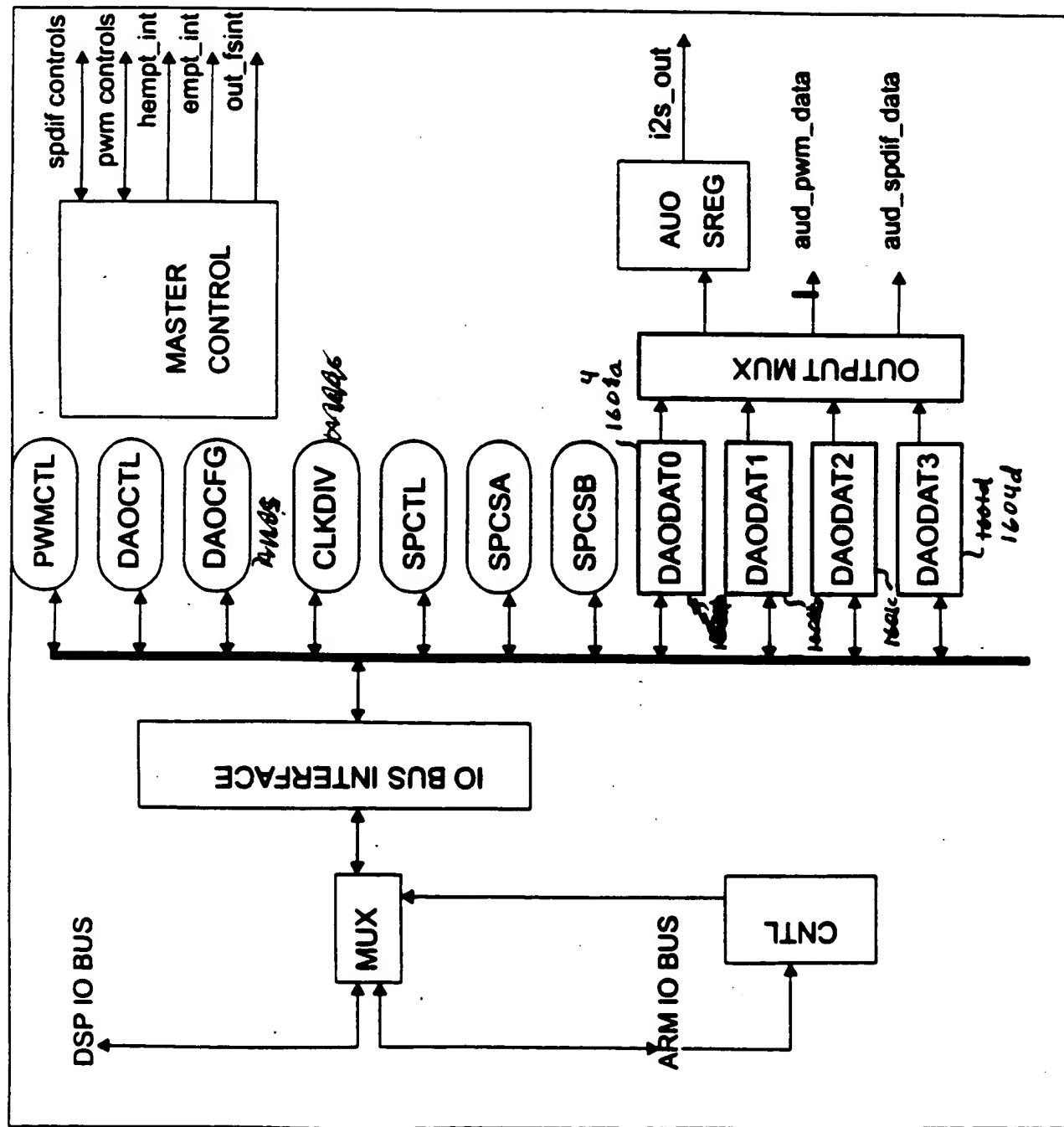


FIG. 16B

FIG. 16C

The following figure shows a typical output waveform.

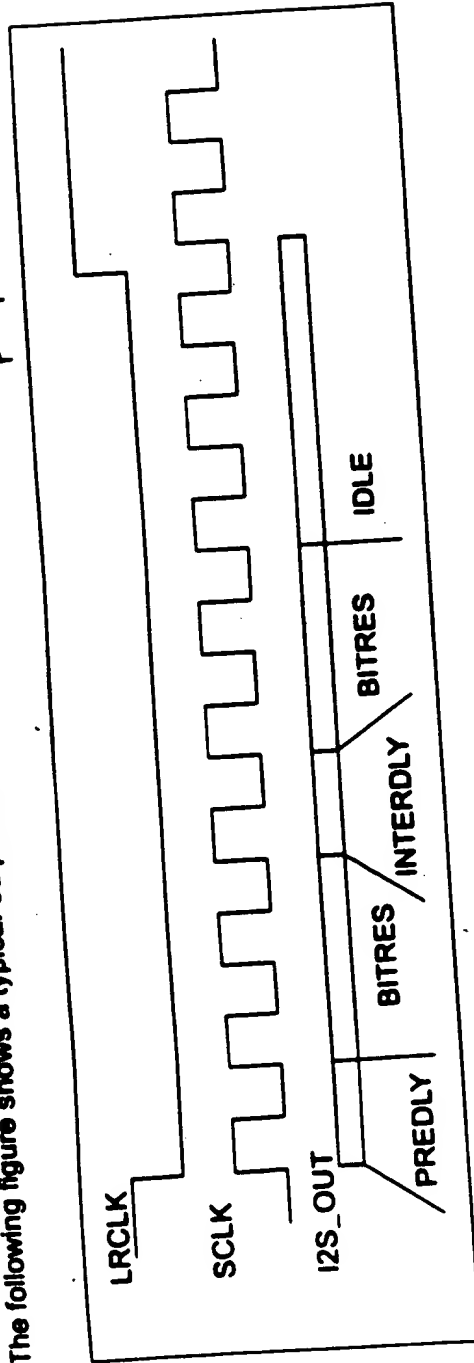


FIG. 16D

1602

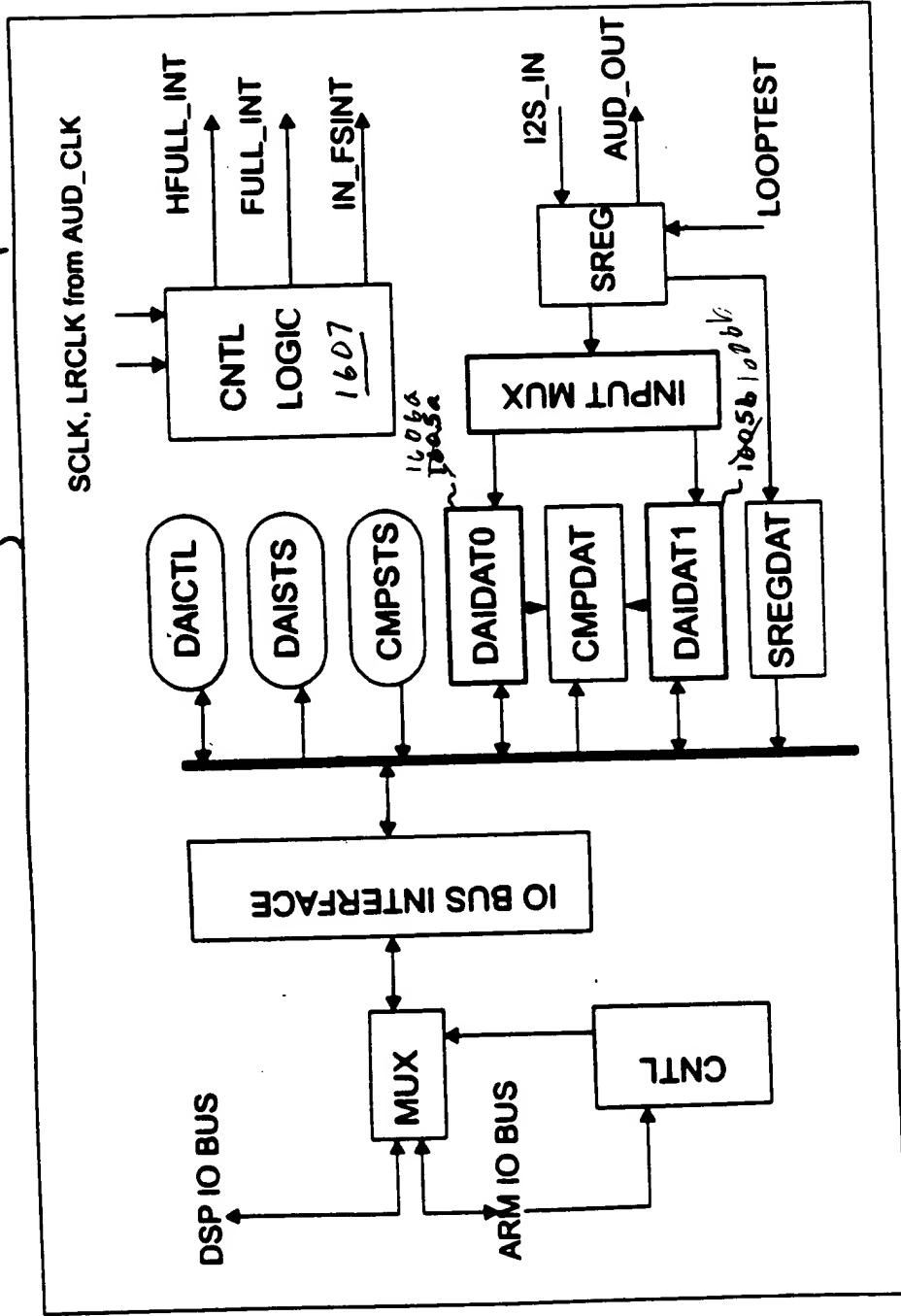


FIG. 17

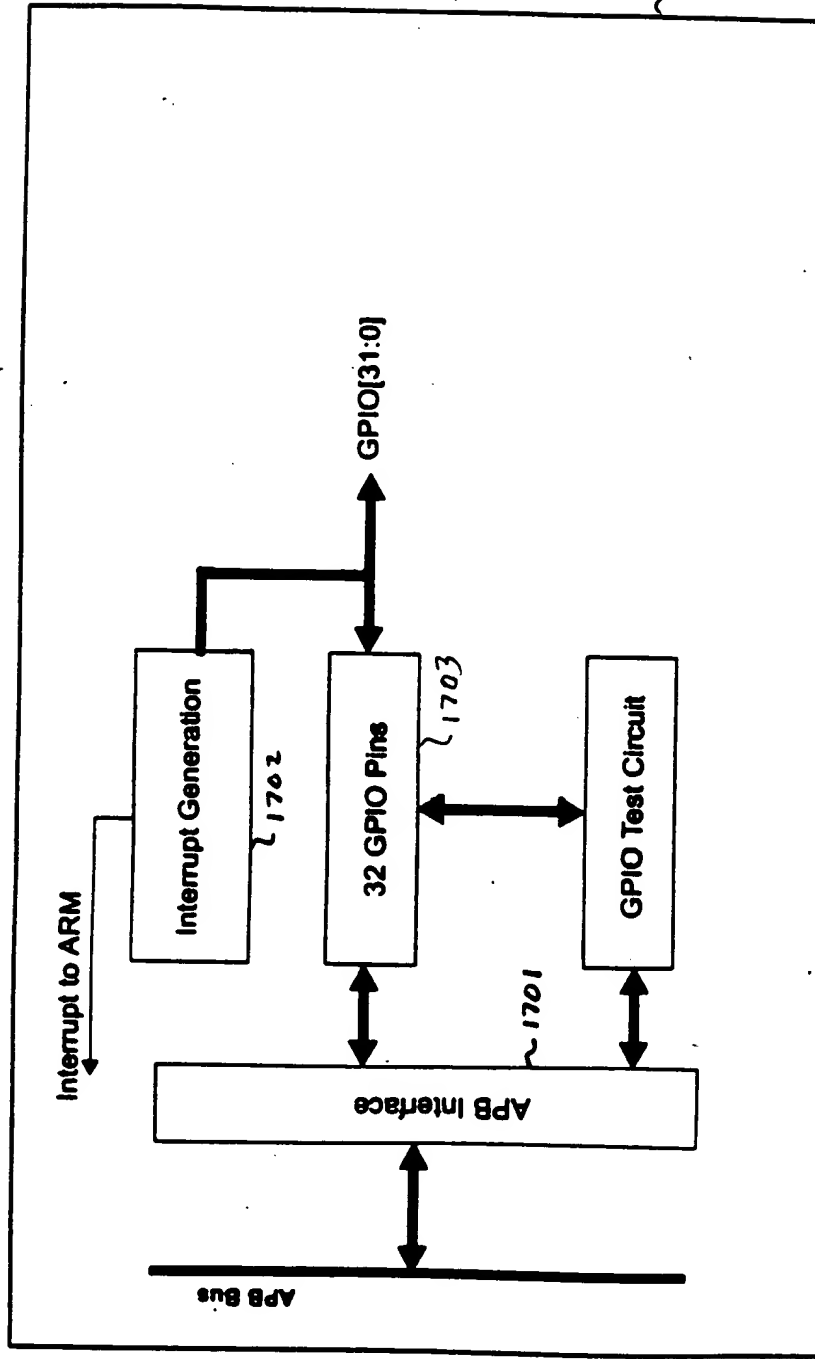


FIG. 18

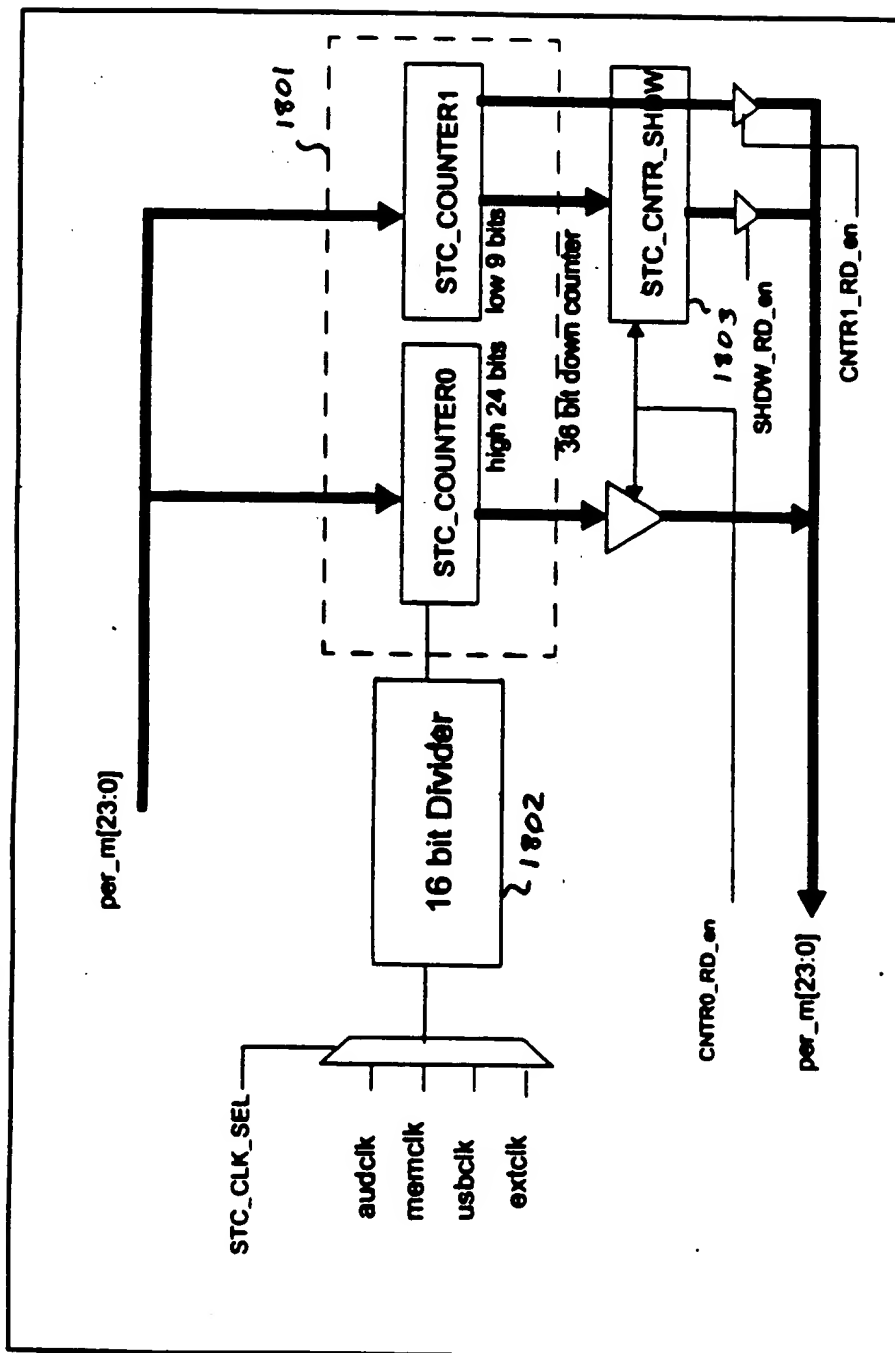


FIG. 19A

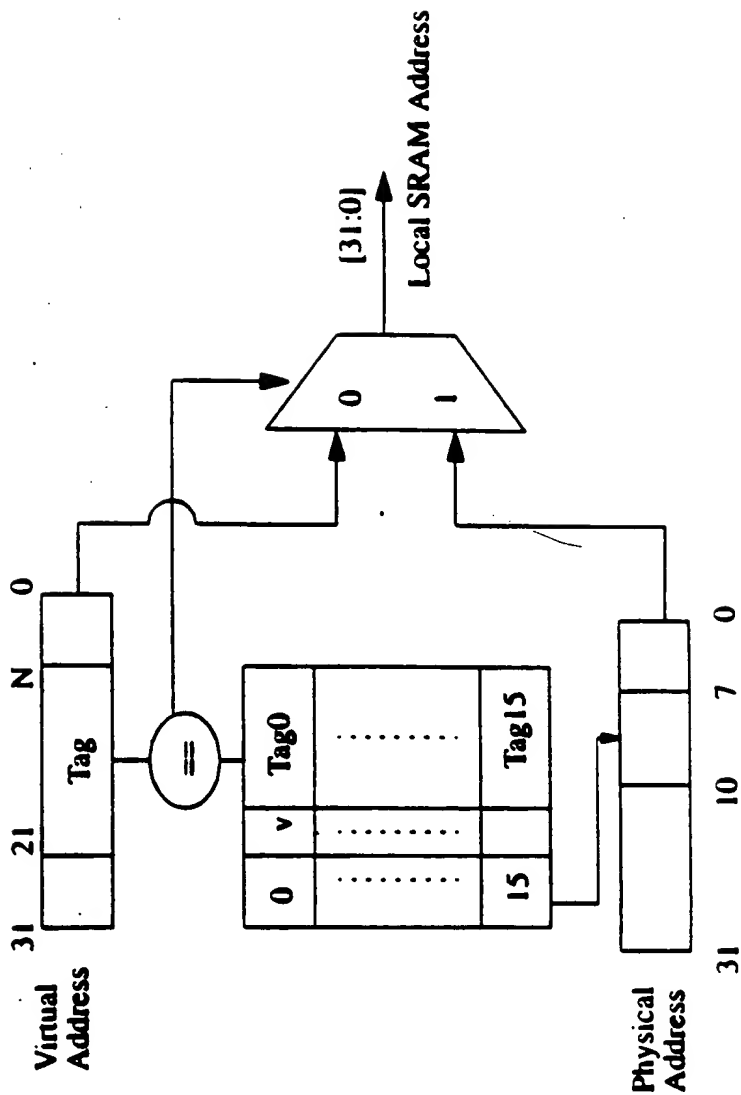


FIG 19B

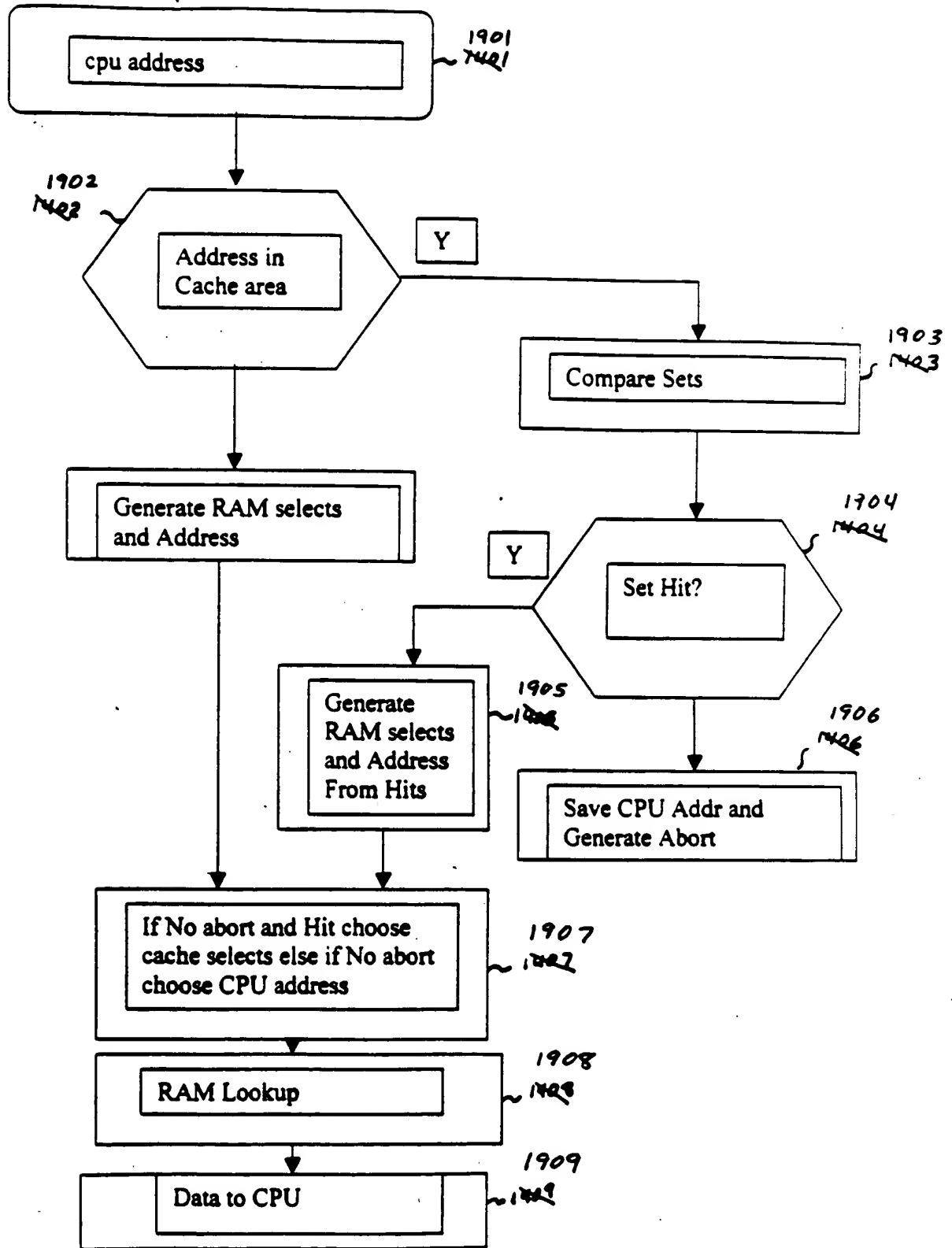


FIG 19B

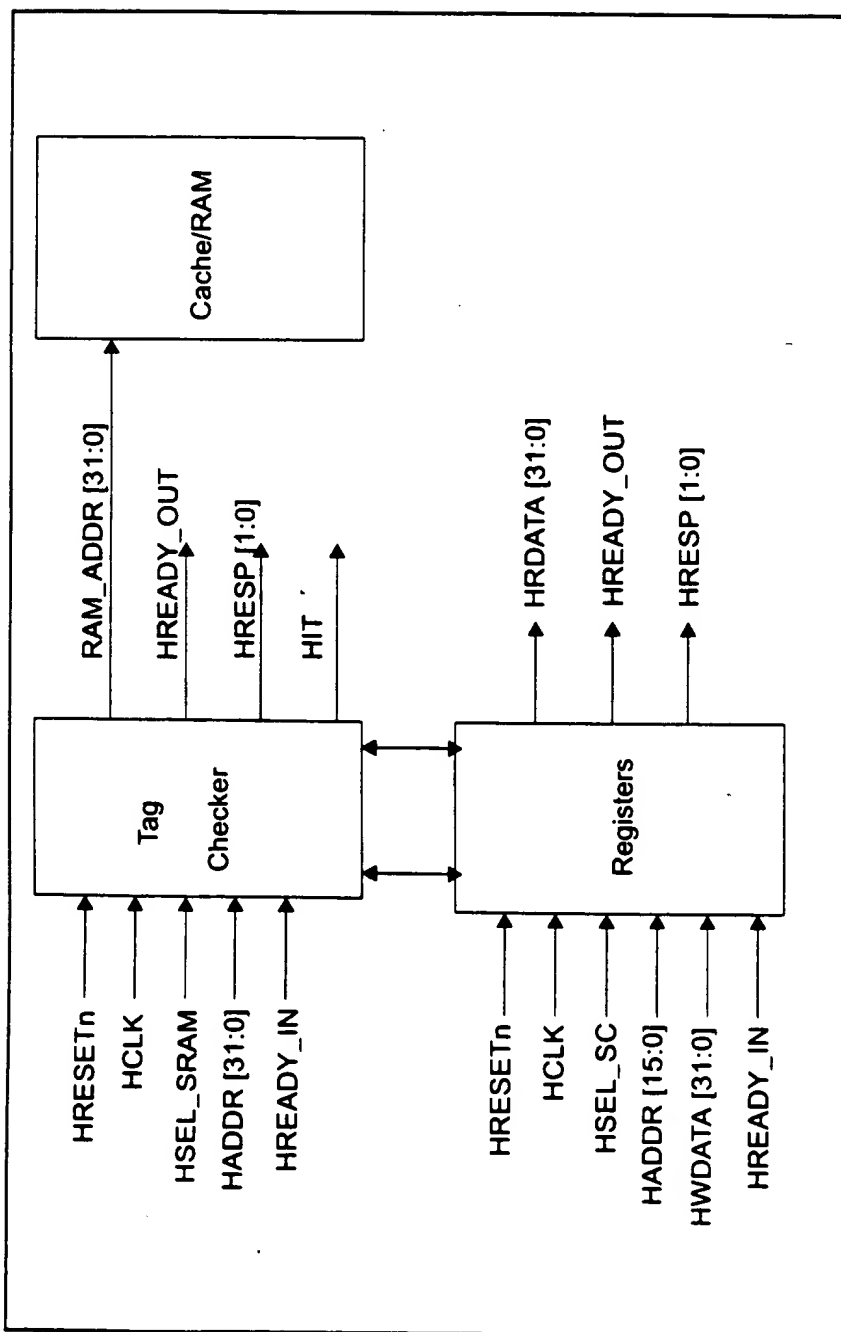


FIG. 19C

Fig. 20A

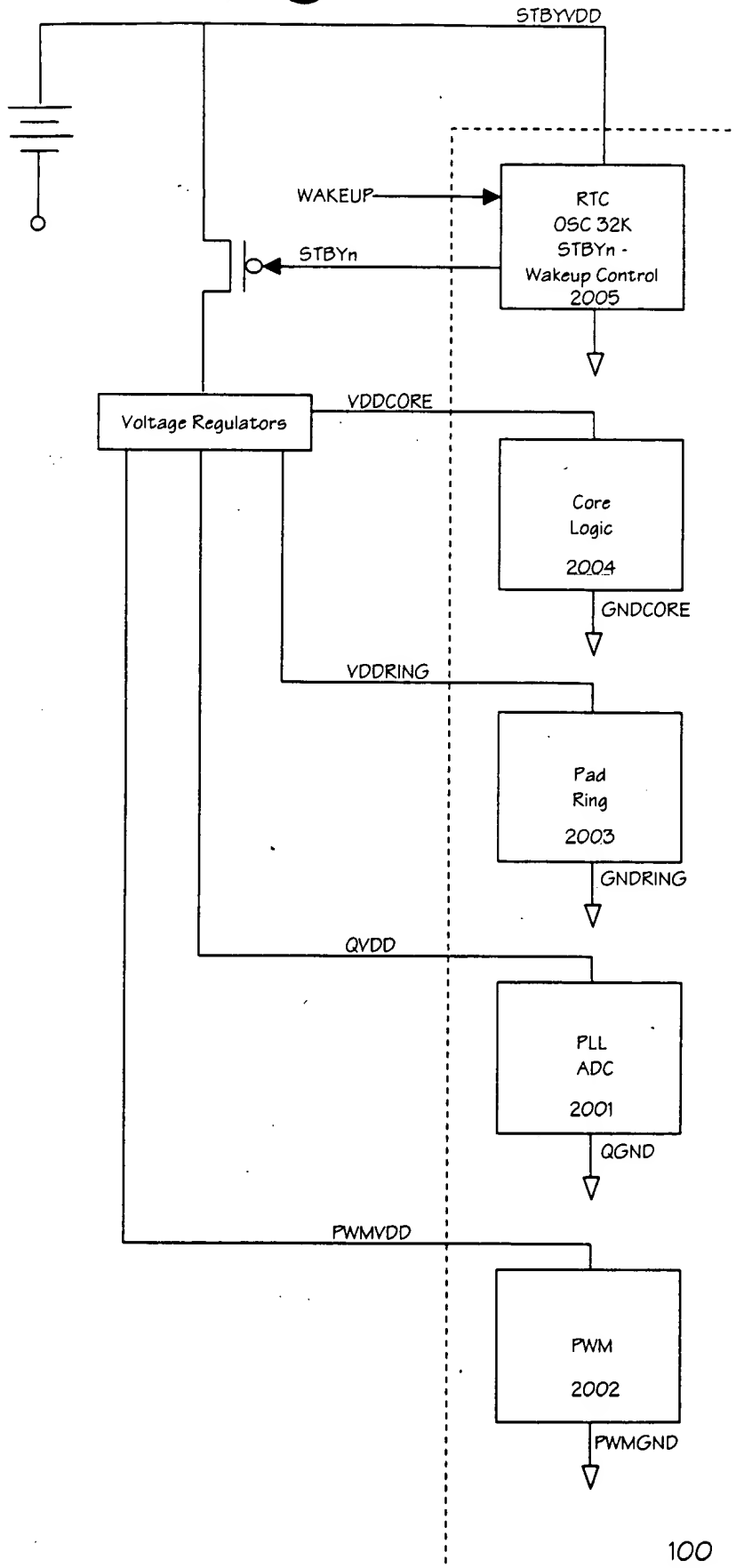


FIG. 20A

FIG. 20B

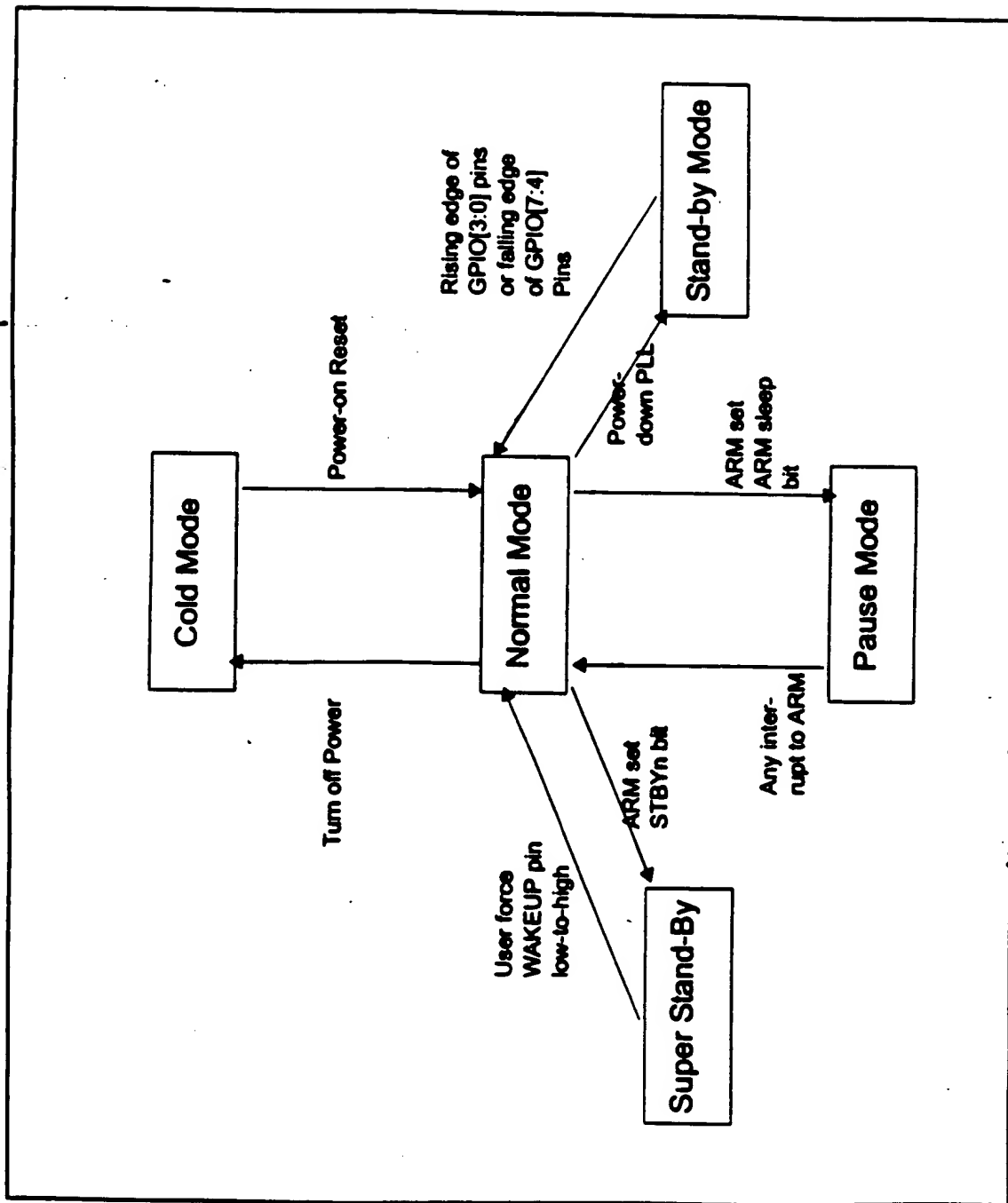


FIG. 20C

Fig. 20C 5
Sheet 1 of 3

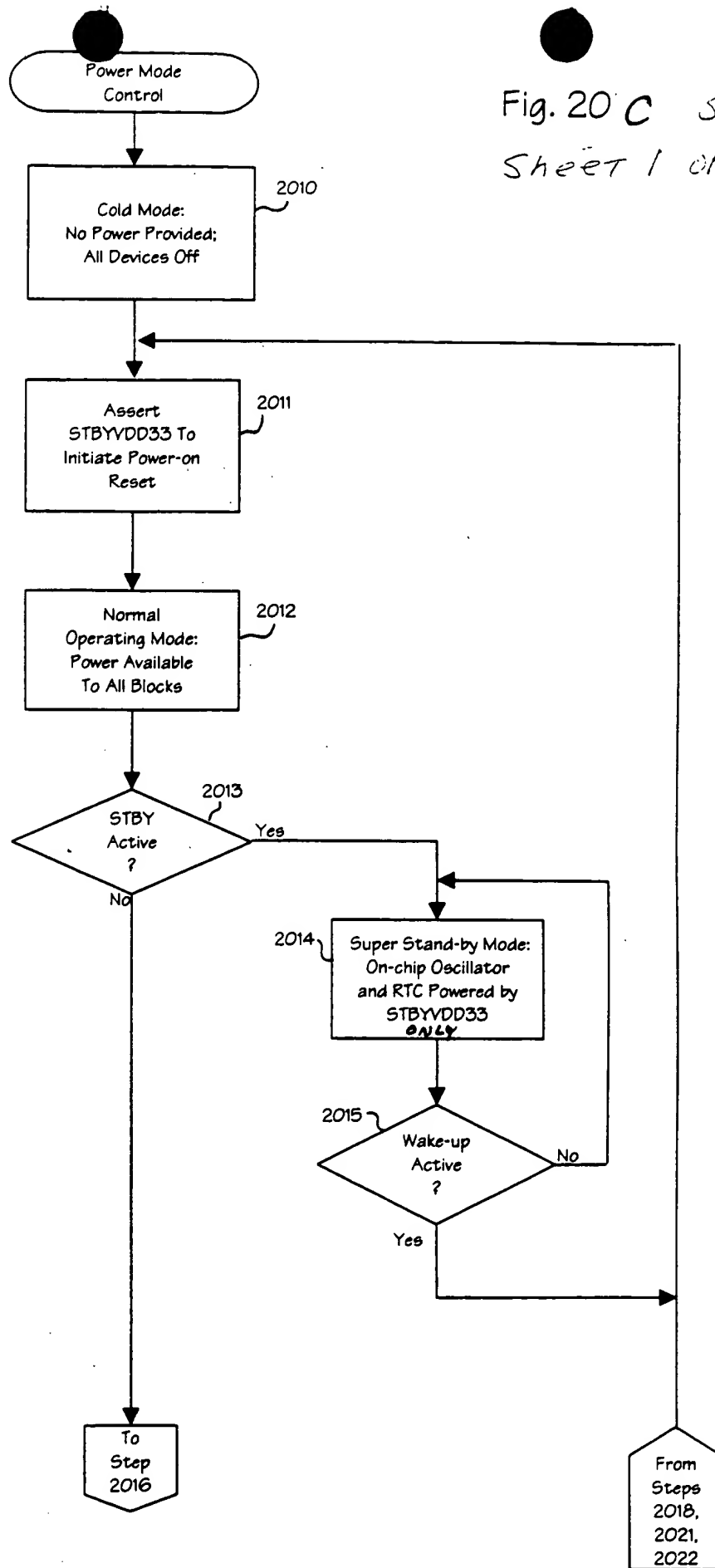


FIG. 20C
Sheet 2 of 3

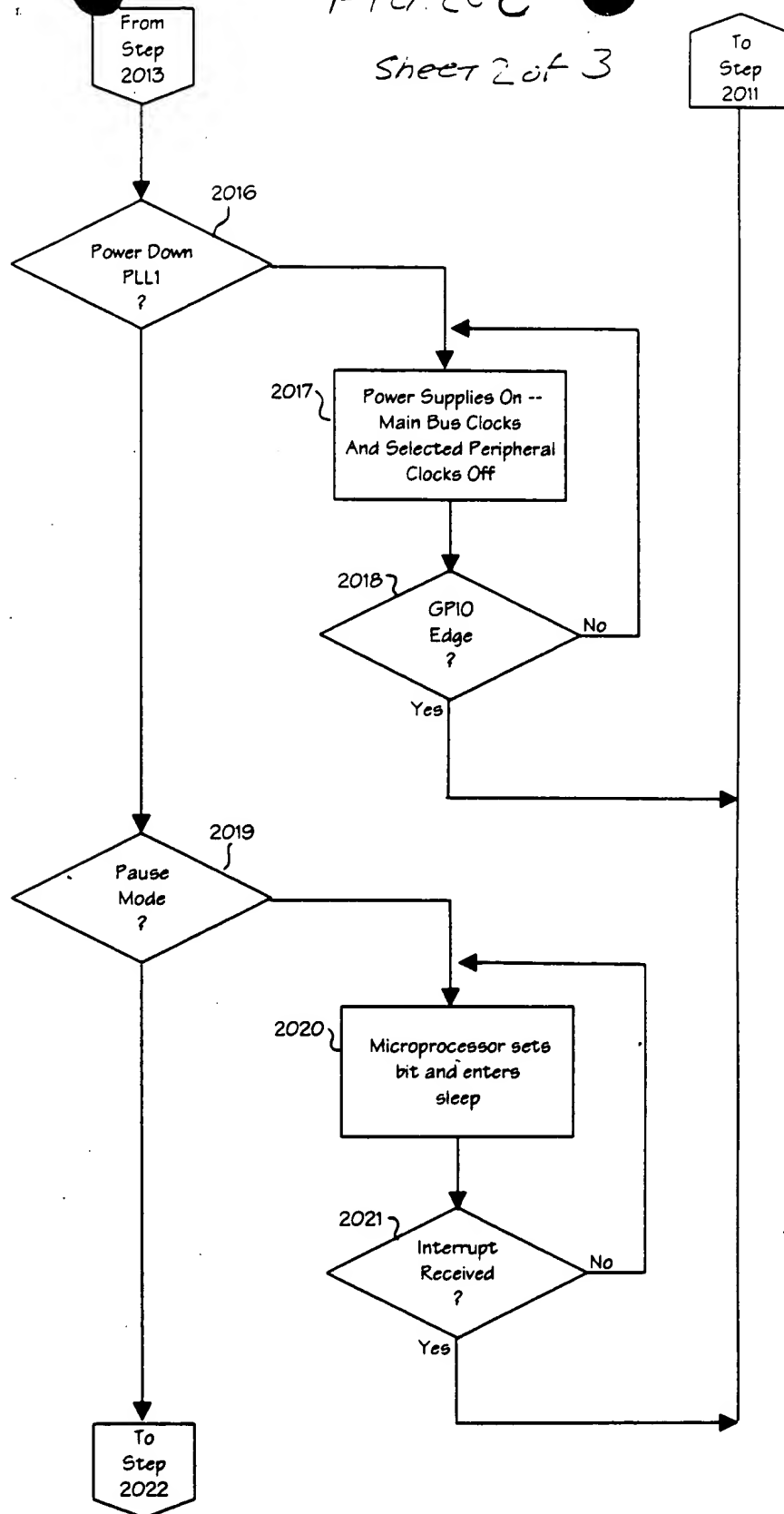


FIG. 20C

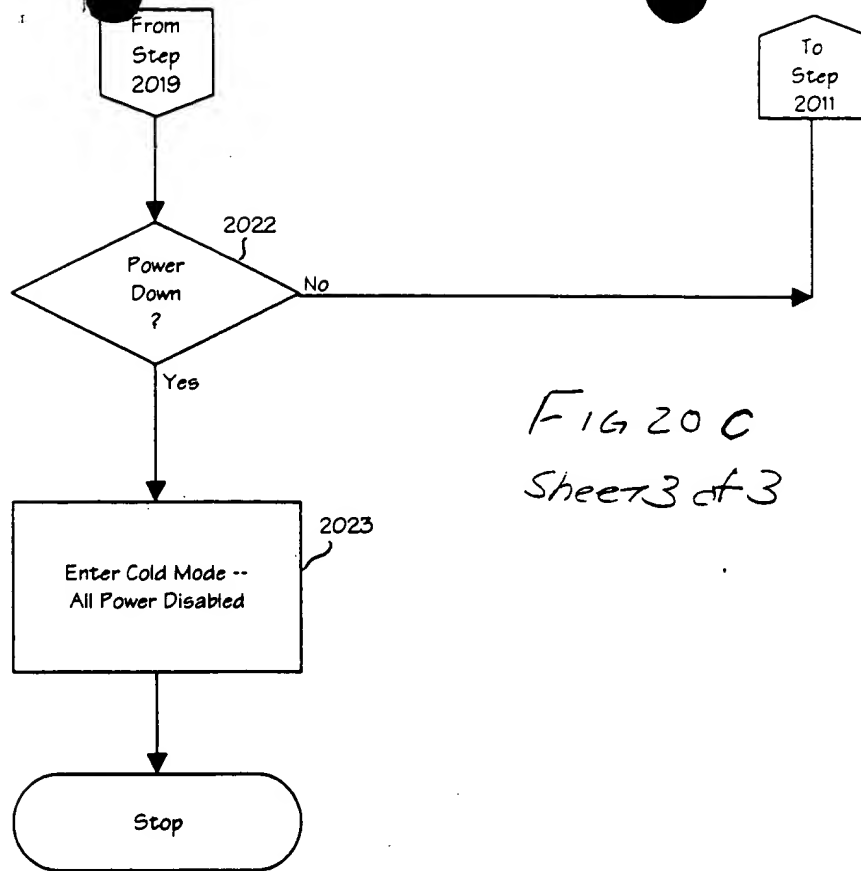
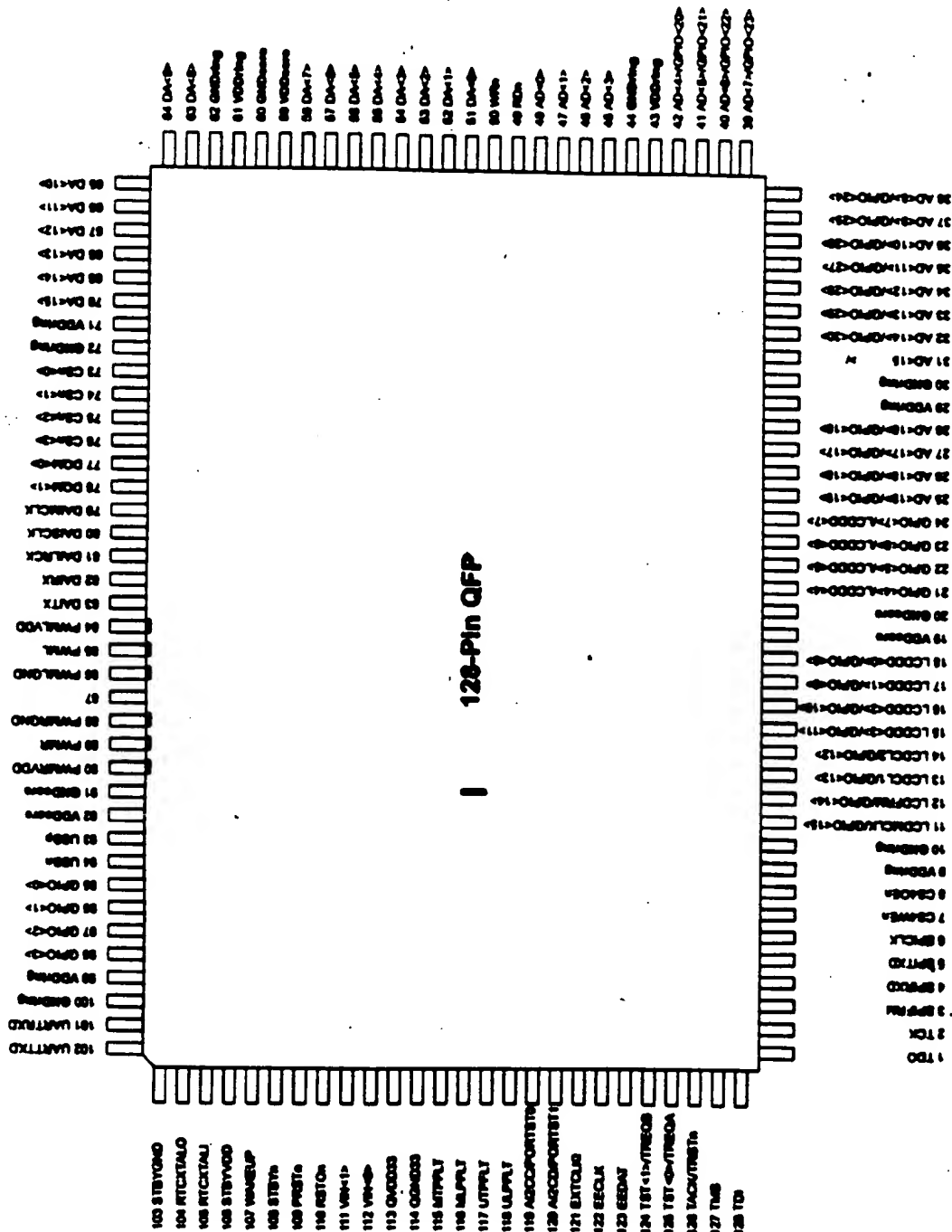


FIG 20C
Sheet 3 of 3

FIG 20C Sheet 3 of 3

FIG 21



* Pins in BOLD are double bonded.
* Some pins are internally bonded which are not shown in this diagram. Please